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IEEE 1558 Brings Precision Time to Mil IP Networks

Tech Focus: MIL-STD-1553 Boards

Volume 9 Number 5 May 2007 www.cotsjournalonline.com

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Compact/Flash	Type I or II	Type I or II	Type I or II
COM 1	RS-232	RS-232/422/485	RS-232
COM 2	RS-232	RS-232/422/485	RS-232/422/485
COM 3	RS-232	NA	RS-422/485
COM 4	RS-232	NA	RS-232
COM 5	RS-232/422/285	NA	NA
COM6	RS-422/485/TTL	NA	NA
LPTI	0	0	1
EIDE	2	2	1
USB	2	6	2
CRT	1600 X 1200	1280 X 1024	1280 X 1024
Flat panel	LVDS	yes	yes
Digital I/O	24-bit prog.	48-bit prog.	24-bit prog.
Ethernet	10/100 Base-T	Dual 10/100 Base-T	10/100 Base-T
Expansion	PC/104 & *Plus*	PC/104 & *Plus*	PC/104
Power	3.6A operating	1.6A max.	1.6A max.
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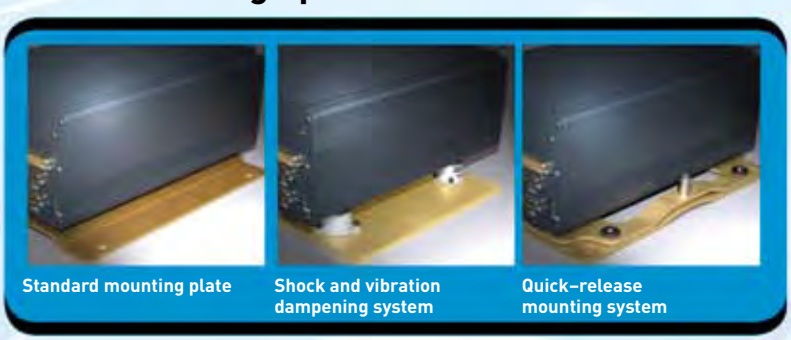

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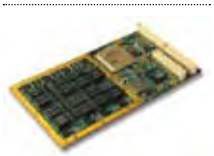

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COTS JOURNAL

Features

May 2007 Volume 9 Number 5

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Multicore for the Military

Tech Recon

Special Supplement: Payloads for UAVs

System Development

Precision Time for Mil Networks

Technology Focus

1553 Boards

COTS (kots), *n.* **1.** Commercial off-the-shelf. Terminology popularized in 1994 within U.S. DoD by SECDEF Wm. Perry's "Perry Memo" that changed military industry purchasing and design guidelines, making Mil-Specs acceptable only by waiver. COTS is generally defined for technology, goods and services as: a) using commercial business practices and specifications, b) not developed under government funding, c) offered for sale to the general market, d) still must meet the program ORD. **2.** Commercial business practices include the accepted practice of customer-paid minor modification to standard COTS products to meet the customer's unique requirements.

——**Ant.** When applied to the procurement of electronics for the U.S. Military, COTS is a procurement philosophy and does not imply commercial, office environment or any other durability grade. *E.g., rad-hard components designed and offered for sale to the general market are COTS if they were developed by the company and not under government funding.*

Departments

Coming in June...

...See Page 73

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The Joint Strike Fighter, or F-35, is a next-generation, supersonic, multi-role stealth aircraft designed to replace aging AV-8B Harriers, A-10s, F-16s, F/A-18 Hornets and U.K. Harrier GR.7s and Sea Harriers. Shown here is the F-35C, which is the U.S. Navy's version of the JSF. More recently, the Lockheed Martin F-35 Lightning II version of the JSF has emerged, designed to satisfy the diverse needs of each of the Service branches.

Courtesy: Lockheed Martin

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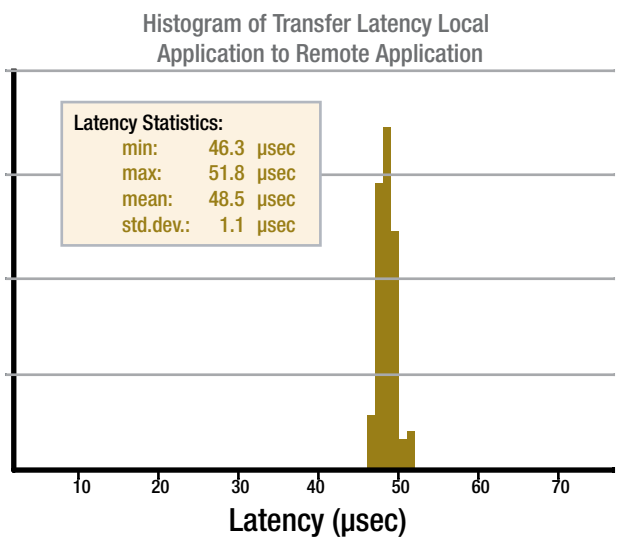

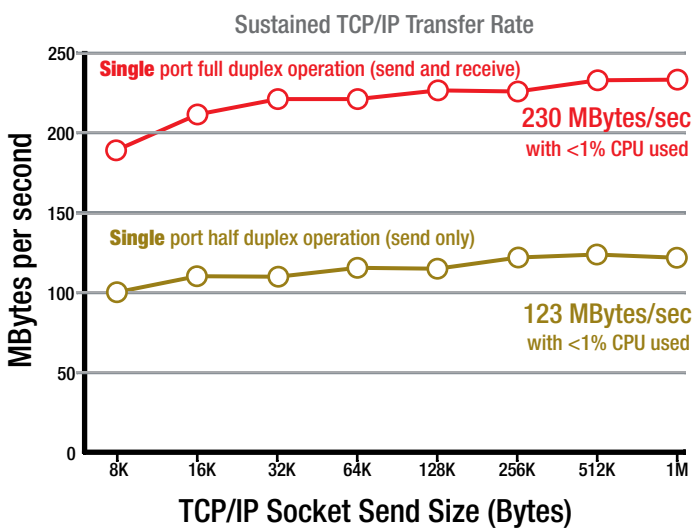

Note: Performance data collected using 1 GHz PowerPC CPUs running VxWorks. All transfers are from CPU memory to remote CPU memory. Latency measured from application send to remote application receive & notification, including Ethernet switch delay.

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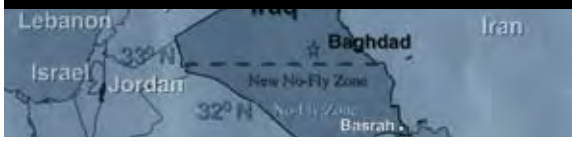

Don't Judge an Invitation by Its Cover

Frost & Sullivan is one of the leading market research and consulting firms with more than 1,500 industry consultants. I've had several opportunities to work with F&S, while representing *COTS Journal* and other organizations, and always with great success. Recently they invited me and several other editors from the RTC Group editorial team to join them at their Excellence in Industrial Technologies Awards ceremonies. What provides a certain uniqueness to these awards is that Frost & Sullivan does research that includes companies ranging in size from 20 people to tens of thousands. They examine firms that are just starting off in the industry as well as those that have been in it for decades.

Truth be told, my first thought was how could I get out of participating gracefully. But as I thought more about it, a string of reasons began to occur as to why I should go. First off, Frost & Sullivan is a dominant industry organization that's been very generous in helping me in the past. I've always found their people extremely knowledgeable. And I have to say that knowledge is reflected in the fact that they found the RTC Group's publications sufficiently influential in the industrial technology market segment to invite us. Unfortunately, Jeff Child, *COTS Journal*'s Editor-in-Chief, was committed to support the military aspect of an RTECC conference in the Boston area and could not go with Warren Andrews, Group Editorial Director, and myself to the Frost & Sullivan event. By the way, Jeff said that RTECC was an extremely well attended event.

In spite of flight delays, cancellations and missed connections due to severe storms at Dallas/Ft. Worth airport, there was a strong attendance. Actually, I think Warren and I were both grateful that everyone didn't make it, giving us more opportunity to immerse ourselves in conversation with the award recipients—which we did from the moment we got there until long after things ended. Not all of the thirty-four award recipients fell into the editorial coverage of *PKG*, *RTC*, *Portable Design* or *COTS Journal*, but a majority did. Not being a technology editor, my focus was more on the financial impact or the potential trends these products and companies will have on the industry. Here are just a couple representative award-winning companies and products:

Cyber Defense Systems, www.cduav.com, received the award for the Best Bang for the Buck. Because of the different roles I've played in the industry, this was probably the most interesting category for me. It's presented to the company that has provided customers with the solution and/or service that provides the highest ratio of value to cost. The recipient is one that has provided customers with a product that boasts quality, while staying extremely competitively priced. Billy Robinson accepted the award for the company's line of CyberBug UAVs. The product line consists of three different UAVs ranging from around 3 pounds to 15 pounds, all priced under $20,000—making them affordable for civilian operations as well as military.

AAI Corporation, www.aaicorp.com, was one of four companies receiving the award for Technology Innovation. AAI received its award for Innovation in Unmanned Aerial Systems. Steven Reid accepted the award for the company's range of Unmanned Aerial Systems—which now includes the Shadow family of unmanned aircraft—and for its One System Ground Control Station. The station is used by a range of UAVs providing the warfighter a singular rather than multiple communication devices to communicate with a wide range of UAVs that may be simultaneously employed.

The Product Innovation of the Year award is presented to companies that have demonstrated excellence in new products and technologies within its industry segment. Winners in that category have shown a keen understanding of the customer needs and have come up with a product that has helped to impact the customers bottom-line positively. This year the award went to four different companies in varying markets. One, for example, was Quintron Systems, www.quintron.com, for its DICES IV product technology. It provided a generational upgrade for the existing Vandenberg AFB Range Status Alert system. This mission control, command center, interoperability and mobile/tactical communication product provided a solution to interoperability and legacy upgrade requirements. David White, Quintron's vice president and general manager accepted the award.

I've only scratched the surface with respect to the products and companies that received awards, and I apologize for not having the space here to acknowledge all of them. My purpose was only to highlight that there are many companies in our industry segment that are diligently working to explore new technologies and provide not only solutions but cost-effective solutions. I'm grateful to Frost & Sullivan for not only recognizing *COTS Journal* and its sister publications as worthy of attending and being part of recognizing the contributions of these companies, but also for their hard work in researching these companies and discovering their achievements. I'm really glad I had second thoughts and decided to attend after all. ▮▮

Pete Yeatman, Publisher
COTS Journal

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The Inside Track

Meggitt Defense Systems Demos Cooling Technology to Army

Meggitt Defense Systems unveiled its latest ruggedized military cooling technologies—featuring its modular Ultra Compact Cooler and Compact Cooler—for the U.S. Army at its Expedited Modernization Initiative Procedure (EMIP) Tactical Wheeled Vehicle Component Demonstrations.

Current and future tactical wheeled and tracked vehicles—as well as sea and air combat platforms—require a significant increase in electronics for command and communications in network-centric joint operations. These electronics, in turn, create a sizable amount of heat. At the event, Meggitt Defense Systems successfully demonstrated a small portable ruggedized refrigeration system (Figure 1a) with 1 kW active cooling to a secondary loop of liquid to directly cool critical electronics and communication equipment without costly upgrades to engines or other systems. The system is designed for internal or external mounting to vehicles. The solution leverages battle-proven M1A2 SEP Main Battle Tank Thermal Management System (TMS) refrigeration technology (Figure 1b) and components to provide portable and flexible cooling without impacting the engine cooling system.

In addition, the small units are designed to support off-the-shelf electronics and are designed with electronics growth in mind. The demo presented similar technologies developed for platforms planned for the Army's Future Combat Systems. Following the demonstration to the Army at the EMIP, Meggitt Defense Systems plans to demonstrate its cooling systems for air and sea applications at various venues around the globe.

Meggitt Defense Systems
Irvine, CA.
(949) 863-0560.
[www.meggittdefense.com].

Figure 1
At an Army TACOM demo event, Meggitt Defense Systems successfully demonstrated a small portable ruggedized refrigeration system (a) to directly cool critical electronics and communication equipment without costly upgrades to engines or other systems. The solution leverages battle-proven M1A2 SEP Main Battle Tank Thermal Management System refrigeration technology (b) and components.

ARINC Engineers Assist U.S. Navy in Growler Aircraft Live Test

A team of electronic warfare (EW) specialists from ARINC Engineering Services, LLC, played a key role in evaluating the next generation of U.S. Navy electronic warfare aircraft—the Boeing EA-18G Growler (Figure 2). A simulated threat emitter was successfully detected, identified and located by the Growler's ALQ-218 Tactical Jamming Receiver, and subsequently jammed by the aircraft's ALQ-99 Tactical Jamming System. The test took place on the Atlantic Test Range near the Naval Air Warfare Center, Patuxent River, MD.

For this first live Growler jamming mission, ARINC's operationally experienced EW professionals used their fleet and T&E backgrounds to assist in evaluating the Growler's EW systems. ARINC and its subcontractor Porter Technical developed test procedures, drafted the flight cards and directed the flight test for the government. The Growler's predecessor, the EA-6B Prowler, is currently used in most U.S. air combat operations, and Navy, Marine and Air Force squadrons are flying the Prowler in support of combat missions in Iraq and Afghanistan. The plane's primary mission is to support strike aircraft and ground troops by interrupting enemy electronic activity and obtaining tactical electronic information within a combat area. The new EA-18G Growler aircraft is expected to perform full-spectrum electronic surveillance and attack of enemy threat radars and communications nets.

Figure 2
On the Atlantic Test Range near the Naval Air Warfare Center, Patuxent River, Maryland, the next-generation U.S. Navy electronic warfare aircraft—the Boeing EA-18G Growler—successfully detected, identified, located and jammed a simulated threat emitter in recent tests.

ARINC
Annapolis, MD.
(410) 266-4652.
[www.arinc.com].

ITT Selects Xilinx Rad-Hard FPGAs for Satellite System

ITT has adopted Xilinx Virtex-II QPro radiation-tolerant FPGAs as a key enabling technology for the Cross-track Infrared Sounder (CrIS). As part of the National Polar-orbiting Operational Satellite System (NPOESS) (Figure 3) and NPOESS Preparatory Project (NPP), CrIS will collect key atmospheric data to allow for improved calculation of temperature and moisture profiles. Forecasters use this type of data in weather models to improve global weather predictions, storm tracking and precipitation forecasts. CrIS provides over 50x the number of information channels and

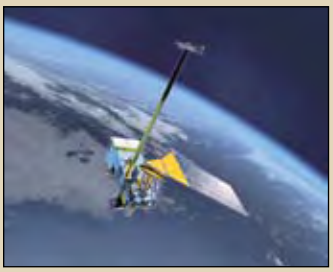

Figure 3

The National Polar-orbiting Operational Satellite System NPOESS is the next-generation low-Earth orbiting environmental data collection and processing system. Northrop Grumman is the prime contractor.

enables up to 3x the accuracy of current systems.

The onboard Xilinx QPro devices enable on-orbit signal processing leveraging dedicated DSP resources that allow 27 channels of concurrent filtering and other processing. The devices are subject to extensive characterization and qualification to an extended temperature range of -55° to +125°C. The family encompasses the latest FPGA families for both military grade and radiation-tolerant applications. NPOESS is the next-generation low-Earth orbiting environmental data collection and processing system. Northrop Grumman is the prime contractor, leading a team in the system's design and development.

ITT
White Plains, NY.
(914) 641-2000.
[www.itt.com].

Xilinx
San Jose, CA.
(408) 559-7778.
[www.xilinx.com].

Saft Rolls Out Lithium Technology for Defense Applications

Saft Space and Defense Division (SDD) has launched a lithium iron phosphate ($LiFePO_4$) technology and presented it at the Advanced Automotive Battery and Ultracapacitor Conference (AABC) jointly with the supplier, Phostech. Saft displayed related data at the Joint Service Power Exposition in San Diego last month. These products use UT licensed $LiFePO_4$ and are available without encumbrances due to intellectual property issues. While potentially beneficial for military use, this is an evolving technology that does not yet solve the problem of calendar life, which is critical for automotive applications and others where life cycle cost is important.

While $LiFePO_4$ cannot match the performance of Saft's $LiNiCoAlO_2$ products, it can provide satisfactory performance in some applications. The interest in $LiFePO_4$ is due to its good thermal stability, which can limit the outcome resulting from severe abuse. Saft's $LiFePO_4$ products will be available in several Space and Defense Division standard formats. Saft SDD is developing standard modules and electronics to make the technology applicable. One of the challenges will be in providing the State of Charge in this technology and in maintaining good balancing of cells.

Saft America
Cockeysville, MD.
(410) 771-3200.
[www.saftbatteries.com].

RGB Spectrum's Display Processors Chosen for LCS Defense System

Raytheon has developed sophisticated operator consoles using RGB Spectrum's RGB/View 7000 multi-image display processors. The consoles are part of Raytheon's SeaRAM Anti-ship Missile Defense System (Figure 4a), an advanced development of the Phalanx system, the most widely used naval defense system in the world. Raytheon, the manufacturer of Phalanx, has developed the new SeaRAM missile defense system that combines the field-proven technology of the original Phalanx system with the Rolling Airframe Missile (RAM) guided missile system.

The SeaRAM system can be equipped with one or two operator consoles, a Local Control Station in the ship's main control center and a Remote Control Station in the ship's Command Information Center. The compact RGB/View 7000 multiple window display processor (Figure 4b) is ideally suited for the console's limited space. It supports the SeaRAM system's thermal imager and combines high-resolution computer and Forward Looking Infrared (FLIR) video inputs in real time. The FLIR integrates multi-spectral thermal detecting and target tracking ability into the system. The SeaRAM system computer provides graphical information, including a range table, target-acquisition imagery and weapons control. To maintain its naval warfighting superiority, the U.S. Navy is building a multi-vessel fleet of lighter, faster ships. The first of these new vessels to be deployed will be the Littoral Combat Ship (LCS), a new

Figure 4

The SeaRAM (a) Anti-ship Missile Defense System is an advanced development of Raytheon's Phalanx system, the most widely used naval defense system in the world. The system uses sophisticated operator consoles that are based on RGB Spectrum's RGB/View 7000 multi-image display processors (b).

family of high-speed, extremely maneuverable, networked surface combat ships.

Raytheon
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(502) 364-6760.
[www.raytheon.com].

RGB Spectrum
Alameda, CA.
(510) 814-7000.
[www.rgb.com].

COTS Websites

www.acq.osd.mil/jctd

Joint Tech Initiatives Converge at Joint JCTD Website

The Joint Capabilities Technology Demonstrations (JCTD) Office, part of the Advanced Systems & Concepts office at the Defense Department, is tasked to exploit mature and maturing technologies and introduces new operational concepts to solve important military problems, and facilitates transition of these new capabilities from the developers to the users. Entering its second year, the JCTD business model replaces the Advanced Concept Technology Demonstrations (ACTD) model in fiscal 2007 to rapidly move advanced technology and innovative concepts into the hands of warfighters in the field.

Building on the successful ACTD model in which new operational concepts are combined with maturing technologies in a joint environment, JCTDs focus more on tailoring projects to a combatant commander's specifically identified needs—emphasizing "needs pull" over historical "technology push." The JCTD tracks the progress of several new Joint Capability Technology Demonstrations. Last month the DoD announced the selection of seven Joint Capability Technology Demonstration (JCTD) projects for fiscal 2007 and three JCTD projects that started at the end of fiscal 2006. Among these are Tactical Service Provider (TSP) for mobile, wireless high-throughput broadband connections over long distances; Joint Multi-Mission Electro-Optical System (JMMES) for counter camouflage, concealment and deception; and Internet Protocol Router In Space (IRIS) for satellite Internet resource allocation capabilities. The JCTD Web site provides access to articles, reports, links to knowledge centers and other resources for all these and other JCTD demos.

Joint Capability Technology Demonstrations, Arlington, VA. (703) 697-6446. [www.acq.osd.mil/jctd].

Special Feature

Multicore for the Military

Multicore Processors Drive Next-Gen Defense Systems

In next-generation, compute-intensive defense systems, multiple compute nodes can tackle huge amounts of data and process it into the forms that warfighters need.

Ann R. Thryft
Senior Editor

In just the last 15 months, multicore processors have gone from being the new kid on the block in military systems to highly probable members of a commercial SBC's component population. The shift to dual-core processors has been swift, and devices with multiple cores have appeared on major leading processor companies' product road maps.

Designers of SBCs in many different form-factors have not waited for this technology to show up first in the world of consumer desktop PCs and go through a lengthy maturation process. Instead, they are placing CPUs with multiple cores on their boards as fast as possible. In particular, boards carrying two or more x86 cores such as Intel's Core 2 Duo are popping up everywhere. Some industry analysts estimate that quad-core CPUs such as Intel's Core 2 Quad and AMD's upcoming quad-core processors will be found in one-third of high-performance desktop systems by the end of this year.

This new generation of multicore processors will help to improve the speed and overall performance of a host of next-generation electronic defense systems, including radar, sonar, SIGINT and UAV control (Figure 1). With multiple cores of the same GPP on one chip, each core can run a separate program thread, the essence of multitasking, which is crucial to signal processing and mission computing applications. Multicore processors are available from a widening number of silicon vendors, including Intel, AMD, IBM and Freescale, as well as Broadcom and PA Semi.

This symmetric multiprocessing approach boosts performance without burning the huge amounts of power that the same number of separate processor chips would consume, and performance per watt is a key indicator for military designs. In the past, shrinking a chip's geometry was the main approach used to increase clock frequencies. But now that those frequencies have risen above 1 GHz and geometries have shrunk to well under 100 nanometers, merely doubling a chip's clock frequency makes power consumption jump by as much as 600% or more. In multicore designs, the shorter signal distances translate into lower power consumption if frequency doesn't change, so speed can increase via the multiple processor cores all running at the same frequency, versus one core running at a much higher frequency.

Figure 1

Multicore processors are tackling data in applications such as radar, sonar and SIGINT and processing it into forms that warfighters can use, as well as improving speed and performance of UAV control electronics. Real-time video sent by a miniature UAV immediately after its launch is reviewed by members of the 407th Expeditionary Security Forces force protection airborne surveillance system team in Iraq.

Courtesy of U.S. Air Force.

A different approach to multicore processing is the tiled design, such as the Cell Broadband Engine (BE) processor, developed by IBM, Toshiba and Sony Group. It includes eight identical, synergistic processing elements in addition to a core based on IBM's Power Architecture. A single Cell BE can deliver up to 64 operations per cycle. Originally created for the video game market, the Cell processor's theoretical peak performance running at 3.2 GHz is more than 200 GFLOPS, or 200 billion FLOPS, especially useful in beamforming and other types of extremely high computationally intensive signal processing.

As the military continues its transformation into a more nimble and information-aware fighting force, high-demand, compute-intensive military systems will need increasing amounts of processing power in ever-smaller spaces. Multicore processors, in all of their varieties, are leading the way. ▮▮

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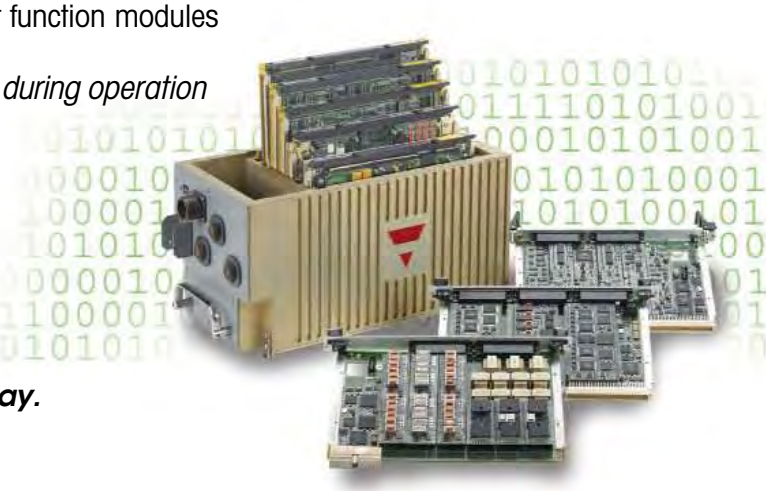

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Special Feature

Multicore for the Military

Riding the Next Wave of Embedded Multicore Processors

High-performance, low-power military systems will be well served by small form-factor design platforms based on multicore processors and symmetric multiprocessing architectures.

Peter Carlston, Platform Solutions Architect
Intel

Why are multicore processors becoming pervasive, even in new embedded military system designs? The short answer is a need for more and more performance.

But many wonder why chip manufacturers are not just releasing faster single-core processors. After all, packing more and more, smaller and smaller transistors into a given space, and running them at faster speeds in every generation, has driven exponential increases in performance for the past 30 years. However, connecting the 200,000,000 transistors of a current processor requires thousands of meters of microscopic "wire," which causes path delays and synchronization difficulties.

In addition, each of those 200,000,000 transistors consumes power and produces heat, and the faster they are clocked the more heat they generate. Leakage current adds to the heat problem, since transistors now measure only three to four atoms wide. In other words, continuing to use single-core processor design methods will eventually result in the processor becoming too hot to cool and internal path delays becoming unworkable.

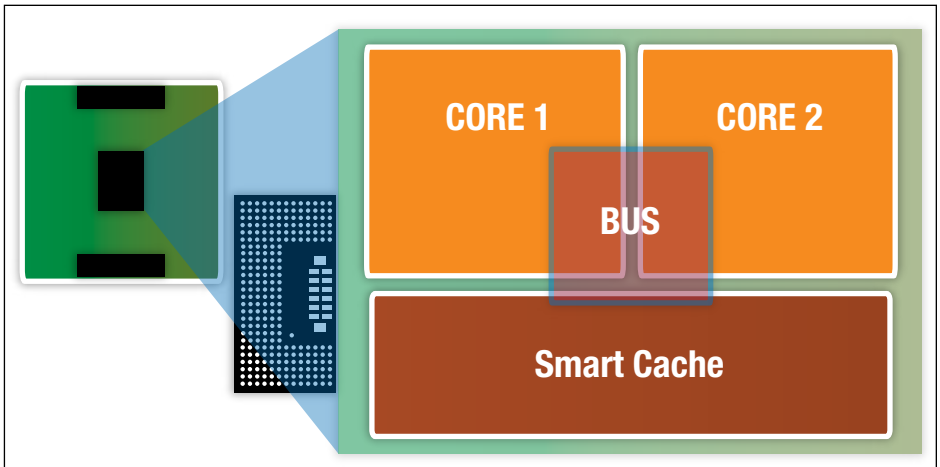

Figure 1

Dual-core processor with mirror-image cores (top) and a 4 Mbyte L2 cache (bottom)

Since reducing a processor's frequency and voltage results in a cubic reduction in its overall power requirements, even small speed reductions can make a big difference. Semiconductor manufacturers have recognized, therefore, that the way forward is to build processors that run at somewhat lower frequencies and voltages, but to integrate two or more of these processing cores on a single chip. Path synchronization issues are reduced since the transistor density and length of conducting paths in each core does not increase as fast.

Overall performance increases because dual processing cores can per-

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form two tasks at once. Of course, transistor designs will continue to evolve. For example, dynamic, ultra fine-grained power gating techniques have enabled Intel's current third-generation multicore processors to achieve impressive performance/watt ratios. Future generations of these multicore processors will use high capacitance process technology to greatly reduce gate leakage current. But from now on, advances in processor capability will derive from advances in multicore processors, not from faster and more complex single-core processors.

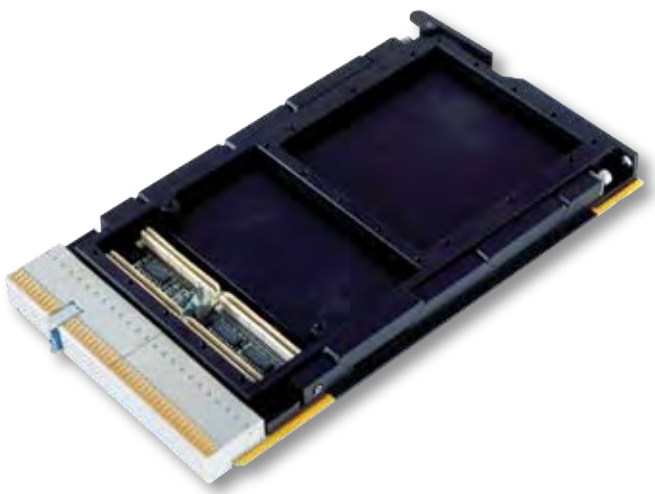

Figure 2

Rugged, embedded SBCs provide small form-factor, deployable symmetric multiprocessing platforms, such as the dual-core 3U CompactPCI Curtiss-Wright Core Duo-based SCP/DCP-1201.

Symmetric Multiprocessing Architectures

Using multiple physical processors on the same blade is not new. Many embedded military applications, for example, have used distributed memory and asymmetric multiprocessing (AMP) architectures for some time. Distributed memory designs effectively place two or more independent processors, each with their own private memory, on the same board.

Asymmetric multiprocessing designs use a symmetric multiprocessing (SMP) hardware architecture, but effectively partition the common global memory between processors, making an SMP architecture appear as a distributed memory architecture to the software. These designs assign work to separate processors, each with its own OS and memory partition within the common global memory. The processors may all be located on the same board, but they are basically separate compute systems that communicate among themselves as needed.

Symmetric multiprocessing architectures are fundamentally different. In these designs, a single block of memory is shared among multiple processor chips or among multiple processing cores on the same chip. A single OS image runs across all cores so that work is done in a truly parallel system. SMP operating systems load-balance work between the available cores.

There is a growing tendency for embedded designers to use these architectures in new designs because of their cost, time-to-market and performance advantages, and SMP has long been the dominant multiprocessing architecture for servers. Software development tools for parallelizing applications are mature, and operating systems such as Linux and Windows have long been highly optimized for SMP architectures.

The hardware and software design issues of SMP are therefore well understood by a large pool of experienced engineers, and this experience can be applied directly to developing multicore SMP systems. Military equipment vendors, for example, have already released AMC and VME boards with dual-core SMP processors, and their roadmaps show even broader SMP offerings in the near future.

Likewise, RTOS vendors are releasing SMP versions of their operating systems and tools, so sophisticated SMP operating system choices are growing. These operating systems have been optimized to automatically balance workloads among all of the available processing cores, thereby maximizing performance and efficiency.

Many multicore processors also include large on-chip Layer 2 caches, which enable very fast data transfers between the cores (Figure 1). It is also easier to hide memory and I/O latency when parallel threads work on different parts of data. These types of workloads also benefit from the multitasking capabilities of all modern processors. Combining multitasking with dual-core multiprocessing, for example, often results in performance gains of 170 to 180% for embedded military applications.

Even though modern multitasking processing cores have very low task switch latency, the delay may be too high for demanding, real-time military data acquisition and processing workloads. Multicore SMP architectures can bring compelling performance benefits for these workloads. For example, an application can utilize "core affinity" techniques so that routine processing occurs on one core, but arriving real-time data is processed immediately on the second core, without the task switch latency that a multitasking single-core processor would exhibit. Other applications may benefit from additional SMP techniques such as flow pinning or data pipelining.

Using SMP Architectures in Military Systems

Several tools are available to help software developers make the switch to SMP designs. For example, Intel's VTune Performance Analyzer, Thread Profiler, Thread Checker and Fortran and C compilers have proven their worth in multitudes of development projects.

Symmetric multiprocessing is suited to many multitasking applications used in today's military systems. Shipboard, ground mobile and airborne systems, such as Unmanned Aerial Vehicles (UAVs), are being designed using multiple, concurrent tasks, which allows more software reuse and better modular designs. Industry standard communications protocols such as Socket and IP traffic simplify task communication. Machines based on SMP architectures are ideal for running multiple components simultaneously. For example, data acquisition, signal processing, telemetry, operator display and control may all be treated as separate tasks when running in an SMP environment.

On a UAV, for example, SMP enables data acquisition, processing and telemetry to be handled as independent tasks. Rugged, embedded boards—such as the dual-core Intel Core Duo processor-based Curtiss-Wright 1201 3U CompactPCI SBC—provide a small form-factor, lightweight SMP processing platform well suited to special requirements of UAVs (Figure 2). Such rugged, multicore SMP boards are well suited for the harsh environments in which UAVs operate, ranging from the extreme heat of a desert runway to subzero temperatures when flying above 25,000 feet, as well as constant vibration and large g-shocks during weapon firings and landings.

A strong emphasis is now being place on next-generation military systems to support a Windows operating system environment to simplify and speed up training for new troops. This trend is helping multicore SMP SBCs find homes in military vehicles where server-class performance is desirable to manage vehicle cargo, maintenance records, parts databases and documentation, as well as provide tracking information to battle commanders.

With the growing demand for performance driving an increased use of SMP architectures, multicore processors offer a good way forward for the computing industry as a whole. For embedded military applications, multicore processors such as the Intel Core Duo are proving well suited for high-performance, low-power systems. ■

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Special Feature

Multicore for the Military

Dual Cores Advance Small Form-Factor Options for Military

With its higher performance per watt and lower BOM costs, multicore processing is being integrated into standards-based, modular, off-the-shelf form-factors optimized for the military's specialized needs.

Christine Van De Graaf, Product Marketing Manager
Cliff Moon, Director of Product Marketing
Kontron

Military systems operate in some of the most sensitive and critical computing environments, such as control systems for weapons, satellite navigation, radar systems for aircraft and ships and communication systems linking soldiers to each other. These types of applications not only demand of computer boards the ability to withstand extended temperature ranges and the high/low pressure changes of high altitude and underwater depths, but severe shock and vibration elements as well.

In addition, for reliable portability new applications require smaller form-factors that offer reduced size, weight and power (SWAP). To compound the challenge, these stringent requirements are often combined with severe time-to-deployment and budgetary constraints.

Faced with these design challenges, developers need the ability to scale solutions and add features within embedded form-factors without dramatically affecting energy variables, such as thermal output and power consumption. Multicore processing platforms have been proven to offer higher compute performance, reduced chip count and lower BOM costs, with drastically reduced

Figure 1

The multicore architecture of Kontron's ETX-CD allows more complex computing needs to be served in the rugged, space-restricted applications where this small form-factor is used.

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Form-Factor	Size (mm x mm)	Key Features	Potential Applications
3U CompactPCI	100 x 160	Compact Size and Weight, Rugged Design	Avionics (such as UAVs), Graphics-Based Ground Applications
ETX	95 x 114	Customizable, Rugged	Avionics, Rugged Computing Platforms (such as UMPCs)
PC/104	90 x 96	Stackability, Passive Cooling	Aircraft Radio and Navigation Systems, Multifunction Displays, Missile Launchers
AdvancedTCA	322 x 280	Fast Bandwidth, Design Flexibility, Open Framework	Next-Generation Carrier-Grade Communications Equipment (such as communication servers)
COM Express	125 x 95	Small, Rugged, Flexible	Unmanned Vehicles, Training Simulators, Portable Tactical Communication Devices
MiniITX	170 x 170	Widespread Availability, Ease of Deployment, Value	Rugged PC Platforms, Network Servers

Table 1

The small form-factors available for military system designs each combine size, performance, power dissipation and price point variables in different ways, and are suited to different applications.

power consumption. As multicore processing platforms become more available, the technology is being integrated into small form-factor boards targeted toward military applications.

Options Abound for Small Form-Factor Rugged Systems

Unfortunately, a one-size-fits-all solution does not exist today. A myriad of different form-factors are currently available, each with its own combination of size, performance, power dissipation and price point variables to consider (Table 1).

Until recently, VME was the solution of choice for high-end military applications. However, current VME designs are unable to meet some of the new applications' demands due to high power dissipation, relatively large size and price points that tend to exceed budgets. To satisfy the need for smaller size and lower cost, a number of standards-based, modular, off-the-shelf form-factors have emerged. They are CompactPCI, AdvancedTCA, Embedded Technology eXtended (ETX), COM Express, PC/104 and MiniITX.

CompactPCI has thrived in military applications, since the limitations of VME-based architectures have been unable to keep up with design requirements. The 6U form-factor has quickly replaced VMEbus in large custom designs. But as the pressure to reduce size and weight intensifies, particularly for Unmanned Aerial Vehicles (UAVs) that carry an increasing array of electronics, the smaller, 3U CompactPCI form-factor is gaining popularity. This form-factor also offers ruggedization benefits due to its significantly greater stiffness, making it less susceptible to shock and vibration.

AdvancedTCA, with its fast bandwidth and design flexibility, has also made significant inroads into military communication applications that are not deployed in the conflict zone. Targeted to the requirements of next-generation, carrier-grade communications equipment, ATCA incorporates the latest trends in high-speed interconnect technologies and next-generation processors, as well as improved reliability, manageability and serviceability.

Embedded Technology eXtended has established itself as a popular, non-backplane form-factor. Targeting customizable embedded requirements,

ETX offers reliable operation and a long life in harsh environments. Since ETX modules employ heat-spreader plates to assist with conduction cooling, they are an option for use in extended temperature ranges as long as the design's components can tolerate harsh environments. These modules have proven successful in avionics where shock and vibration are among the most important design issues.

Many space-restricted applications can benefit from the small, space-saving design of an ETX CPU module. Boards designed to this form-factor, specifically the ETX-CD and ETX-PM derivatives, have also proven to be well suited for custom designs involving computing modules in mobile platforms (Figure 1).

ETX modules have also been successfully implemented in a rugged, ultra-mobile PC (UMPC)-based system that demanded a modular solution with great flexibility. The small, rugged and portable device was designed quickly using a semi-custom solution along with custom BIOS. In this application, ETX modules provided maximum performance that allowed the mobilized system to fulfill the demand for mission critical, high-end computing.

Small and rugged computer-on-module implementations are ideal for a broad range of embedded applications where they fit mechanically, economically and functionally, and where other form-factors such as add-in cards cannot be used. High-performance systems can use COM Express to help transition designs that rely on legacy bus technologies to future-focused technologies such as PCI Express and Serial ATA. The form-factor flexibility of COM Express, with its five pin-out types, enables developers to segment their designs for different classes of embedded applications. Applications such as unmanned vehicles, training simulators and portable tactical communications devices can all benefit from COM Express.

Another worthy contender for military applications is PC/104 as it provides strong connectors in a small, stackable and extremely rugged design. The stacking PC/104 bus is an exceptionally strong mechanical interface that creates a solid connection between the board, or stack board, and the system. In addition, many PC/104 designs facilitate passive cooling, eliminating moving parts and increasing reliability. Areas that can take advantage of PCI/104 include aircraft radio and navigation systems, multifunction displays and missile launchers.

MiniITX SBCs offer a combination of value, widespread availability, feature choice and ease of development. Extreme temperature swings, high-vibration situations and deployments lasting

five or more years still challenge MiniITX boards. However, MiniITX has recently begun to show up in more robust solutions, such as harsh environment PCs. This is because both fanless and solid-state systems are easy to create in this form-factor, due to its low power and low heat characteristics.

Multicore Processing Adds Performance, Cost Benefits

Multicore processing can deliver much needed increased performance-per-watt to provide greater processing per square inch, while reducing the associated costs and risks of implementing new technologies. The first multicore architecture from Intel is an example of a power-sensitive blueprint design providing enhanced energy-efficient performance to help balance processing capabilities within power and space constraints.

In order to take full advantage of multicore processing performance, both the operating system and applications running on the computer must support thread-level parallelism (TLP). Dual-core processing—combined with Intel Hyper-Threading technology (HT), which allows one core to function as two logical cores—enables vast increases in the amount of work a processor can do in the same amount of time as a single-core processor. With HT technology, one dual-core processor can simultaneously run four software threads. As more processors are added to a server, the number of supported threads increases to help deliver even better overall performance.

Another important feature is Intel's virtualization technology, which allows multiple operating systems and applications to run as virtual machines in independent partitions on one platform. This makes the overall system more stable because processes that would collide on single-core systems can be separated. It also helps reduce cost considerably by eliminating the need to use expensive engineering resources to modify legacy code in order to take advantage of multicore architectures.

Small form-factor computing holds a promising future in rugged military system design. The number of options that can stand up to these systems' demands have increased, resulting in multiple varieties of technology, performance and size to choose from. As new technologies such as multicore processing come to market, an even larger number of more powerful options will be available on the horizon. ■■

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Special Feature

Multicore for the Military

Multicomputer Programming, Cell BE Processor Boost Signal Processing

The high performance levels of multicore processing, combined with multicomputer programming techniques, are delivering the computationally intensive signal processing required in many defense electronics systems.

Tom Roberts, Product Marketing Manager
Mercury Computer Systems

Many defense electronics systems require the support of certain types of computationally intensive signal processing for operations, such as beamforming. Beamforming is a signal processing process critical to advanced applications such as Space Time Adaptive Processing techniques in radar and many signals intelligence applications. Beamforming manipulates multiple data pulses, from multiple antennae and/or multiple time slices, to increase the magnitude of a signal in a desired direction and decrease the magnitude of unwanted signals, or noise, received from all other directions.

The high performance levels of multicore processing, combined with multicomputer programming techniques, deliver solutions that are extremely well suited to these types of computationally intensive signal processing. In particular, the Cell Broadband Engine (BE) processor is a leading example of the performance advantages inherent in a multicore architecture. The Cell BE consists of one IBM 64-bit Power Architecture core, called the power processing element (PPE), and eight specialized coprocessors called synergistic processing elements (SPEs) (Figure 1). These nine cores, in addition to external memory, are connected via the high-performance element interconnect bus (EIB). The SPEs deliver the Cell BE's processing power using a novel single-instruction, multiple-data (SIMD) operating architecture.

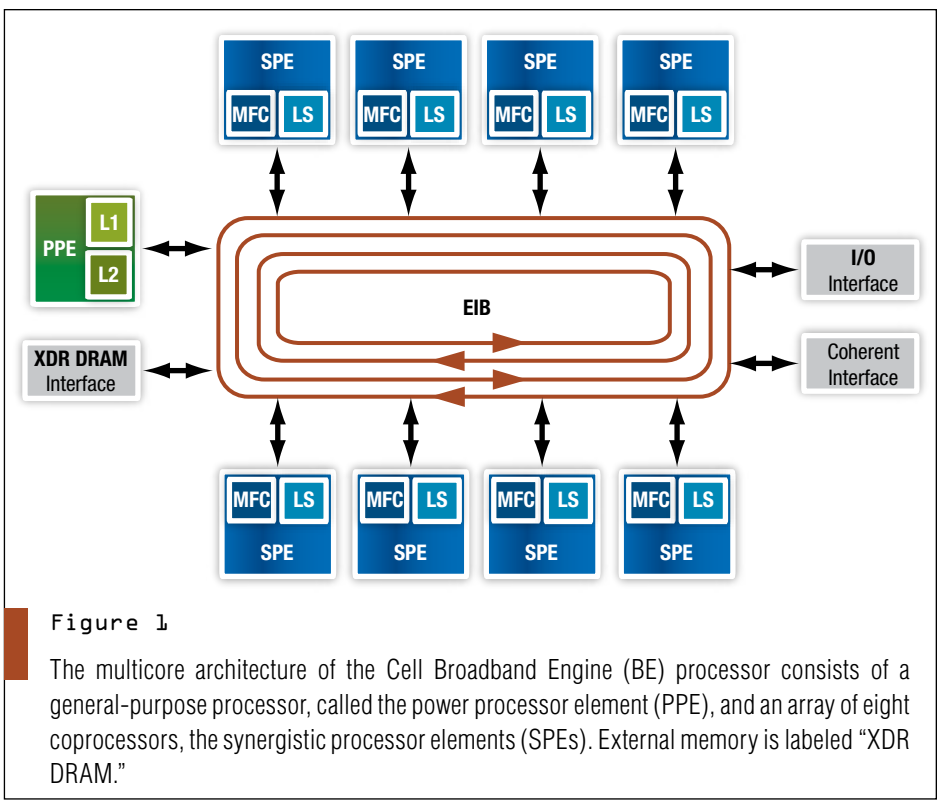

Figure 1

The multicore architecture of the Cell Broadband Engine (BE) processor consists of a general-purpose processor, called the power processor element (PPE), and an array of eight coprocessors, the synergistic processor elements (SPEs). External memory is labeled "XDR DRAM."

The SPEs are oriented toward parallel-vector processing, that is, the coordinated processing of a single data set by multiple processors. Each SPE contains a synergistic processor unit (SPU), a memory flow controller (MFC) and 256 Kbytes of local store (LS), used for both the SPU's code and data. The MFC consists of several DMA engines that can be used to transfer

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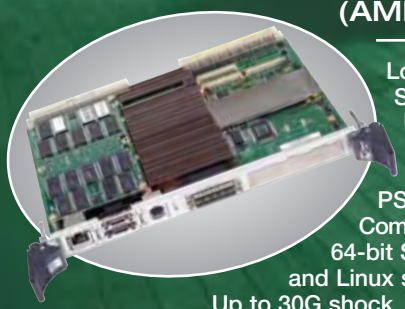

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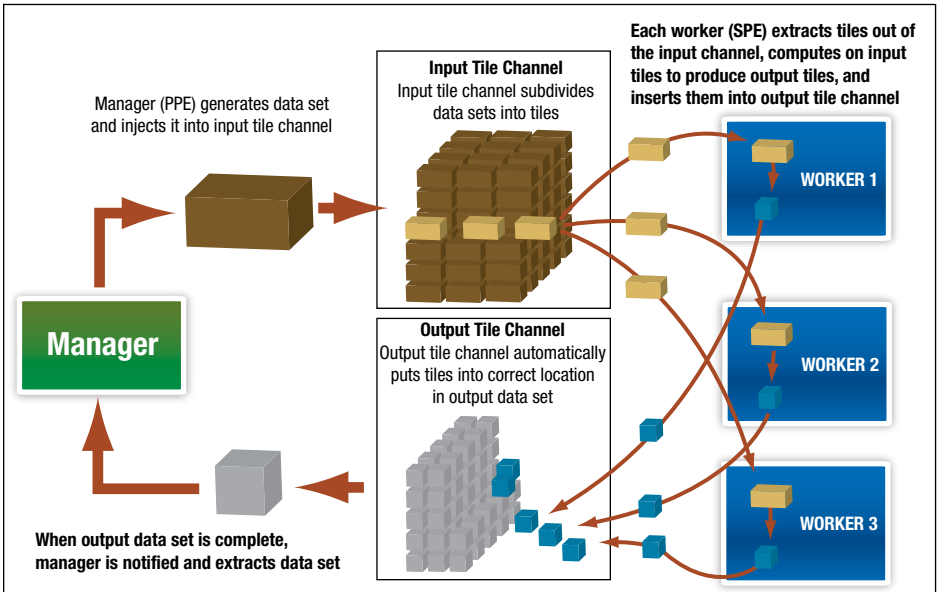

Figure 2

The MultiCore Framework software tile channel facilitates communication and data movement between a manager core, the PPE, and the worker cores, the SPEs, for lower latency and efficient resource utilization.

data or code across the EIB from/to the SPE's LS to/from either external memory or the LS of any of the other seven SPEs.

Each SPU contains a 128-bit-wide SIMD engine. Its four-way, 32-bit fixed and floating-point instructions are capable of delivering up to eight operations (four multiply-accumulate instructions) per cycle, per SPU. Thus, a single Cell BE, using its eight SPEs, can deliver up to 64 operations, or 32 multiply-accumulates, per cycle.

The resulting theoretical peak performance for a Cell BE running at 3.2 GHz is an impressive 204.8 GFLOPs. True application performance is, of course, less but still on the same order of magnitude. For example, optimized, complex, single-precision FFT algorithms have been shown to operate at 176.8 GFLOPs for an 8K FFT and 90.8 GFLOPs for a 64K FFT.

This high level of performance, combined with its orientation toward parallelism, makes the Cell BE processor extremely well suited to beamforming and other types of computationally intensive signal processing required in many defense electronics systems.

In addressing a beamforming algorithm, the Cell BE processor can bring its multiple vector processing engines to bear on the multiple data pulses. The challenge lies in the complexity of programming these types of operations. First, there is the problem of distributing the processing efficiently across the multiple cores. Second, there is the problem of managing the use of a multilevel memory hierarchy not based on traditional cache hardware.

Multicomputer Programming and the MultiCore Framework

Mercury's MultiCore Framework is a suite of software tools and libraries that addresses both issues. It functions as a middleware, simplifying the task of developing embedded software for the multicore Cell BE processor without sacrificing performance. It uses a multicomputer programming model in which a manager core, the PPE, acts as the operations controller while multiple worker cores, the SPEs, act as mathematical processing engines (Figure 2). This middleware also uses two abstractions, tiles and tile channels, to help programmers map their application processing and input data onto multiple cores.

The manager-worker programming model—also known as the function offload engine model—gives the application developer the flexibility to use the MultiCore Framework to implement a wide variety of applications. The library includes functions for the manager, the PPE, and the worker, the SPE. A developer writes the manager side of an application using the manager API and

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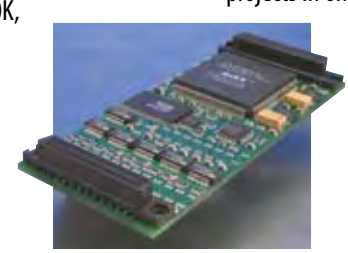

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one or more complementary processing programs for the worker side using the worker API. The manager automatically loads the worker kernel when operations are initialized. Another way to describe this programming model is to say that the manager (PPE) runs the control plane code while the workers (SPEs) run the processing plane code.

With this programming model, the key to optimal performance is keeping the worker cores continually fed with data for processing. To accomplish this, data tiling and tile channels are used. An input data set is described as a multidimensioned matrix, broken into small chunks, or tiles, by the manager program. The manager defines the number of dimensions of the data set, the size of each dimension of the data set, and the size of each dimension of a tile, as well as other applicable parameters.

Another abstraction, the tile channel, is used to move tiles to or from the workers. Once the data matrix has been defined by the manager program, the worker simply connects to the tile channel and thereby obtains the prescription for DMA transfers that move data into or out of the local store. If desired, application code in the worker can inspect the tile descriptor to learn the tile dimension, size and other tile-specific parameters.

The worker program takes one tile buffer at a time from the input channel. While it owns the buffer, the worker program is free to perform whatever math operations are required by the algorithm. Once it has no further use for the data in the buffer, it returns it "empty" to the tile channel. At this point, the tile channel implementation is able to issue a DMA command to pre-fetch the next tile into SPE local store.

This repetitive operation results in a "strip-mining" of data, moving data in successive chunks from external memory into the LSs of the SPEs. It allows for concurrent I/O and processing while minimizing the amount of system-level code that must reside on each SPE. The output channel operates in an analogous manner: the worker program obtains an empty tile buffer, fills it and returns it to the channel.

To support data reorganization, such as global matrix transpose, the middleware also supports the concept of "reorg" channels, which are similar to tile channels. Applications can perform multi-buffered, many-to-many, n-dimensional data reorganizations among sets of workers (SPEs) via reorg channels.

The concepts and approach of the MultiCore Framework will appear familiar to application programmers who have had to maximize the efficient use of the cache memory hierarchy of conventional processors. Now they have explicit control over how data and processing is divided up among multiple cores and LSs, while being insulated from specific hardware details. This middleware is allowing such programmers to exploit the power of the multicore Cell BE processor. ▮▮

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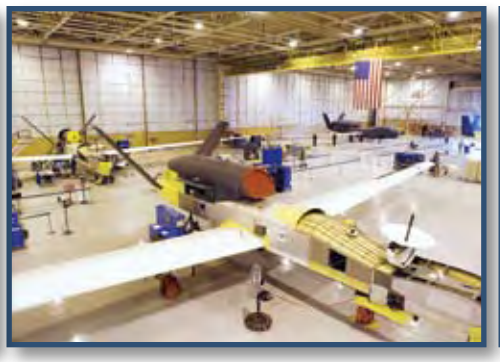

SPECIAL SUPPLEMENT

Tech Recon

Payloads for UAVs

UAV Signal Processing Payloads Push Compute Density Curves

Advances in FPGAs are resulting in dramatic jumps in signal processing compute density. UAV signal processing payloads are reaping the rewards of that integration, but fragmentation of platform designs remains a challenge.

Jeff Child
Editor-in-Chief

The signal processing aspects of UAV payloads—radar, signal intelligence (SIGINT) and communications intelligence (COMINT)—perhaps more than any segment of UAV design—are enjoying dramatic boosts in capability thanks to embedded board-level computers and subsystems. For reconnaissance UAVs like the Global Hawk (Figure 1), the goal has been toward gathering information, not just data.

Consider just the simple cases of a UAV using radar to capture a strip map, or a UAV with an Electro-Optical payload that is scanning the ground. Those activities generate tremendous amounts of data and at fast rate. Embedded processing technologies are enabling fairly intelligent reduction of that data while in the air, converting it into information useful on the ground.

Gone are the days when recon aircraft collected data that had to be brought back to the ground, where a mainframe computer reduced the data into imagery. In today's UAVs, image formation is done in the air and then sent down. "For payloads of the future, including Multi-INT payloads," says Jon Lathrop, market segment director at Mercury Computer Systems, "the trend is toward fusing data and sending down just things that are different than the established data base—or some other way of compressing and fusing the information." Multi-INT is the collaboration of two or more intelligence disciplines, such as SIGINT, COMINT and GEOINT. All of this helps overcome the defining constraint for these systems: the limitations of data link bandwidth.

FPGAs Drive System Integration

The technology that's enabling this boost in embedded compute density is the advance of large, powerful FPGAs with signal processing functionality. Next-generation UAVs are replacing the multiprocessing of big, power-hungry PowerPC-based boards, with more integrated boards with FPGAs. "We're seeing FPGAs have an absolutely massive impact on UAVs," says Mike Jadon of Micro Memory. "The whole idea of shrinking these platforms down is really only possible because of FPGAs. To get that processing otherwise would require a ton of PowerPC Altivecs." Where the original Global Hawk embedded around 40 boards, today's system has replaced around 30 of those boards with just a handful of FPGA-based cards.

That dramatic trend in integration is due to the way that FPGAs process DSP-kinds of functions for radar and SIGINT. According to engineers involved in the project, when the Global Hawk used a multicomputer based on PowerPC Altivecs, a lot of its processing was dedicated to "stupid"—in other words repetitive—functions. Operations like repetitive convolutions—essentially data reduction and manipulation—all totaled occupied around 75% of the processing muscle of the system. In contrast, the data-dependent "intelligent" operations—which general-purpose processors like the PowerPC are good at—occupied a much smaller portion. Concurrent with the advent of more powerful FPGAs, the latest and greatest Freescale PowerPCs have come on line with faster memory bandwidth, further helping to shrink the embedded computing requirements.

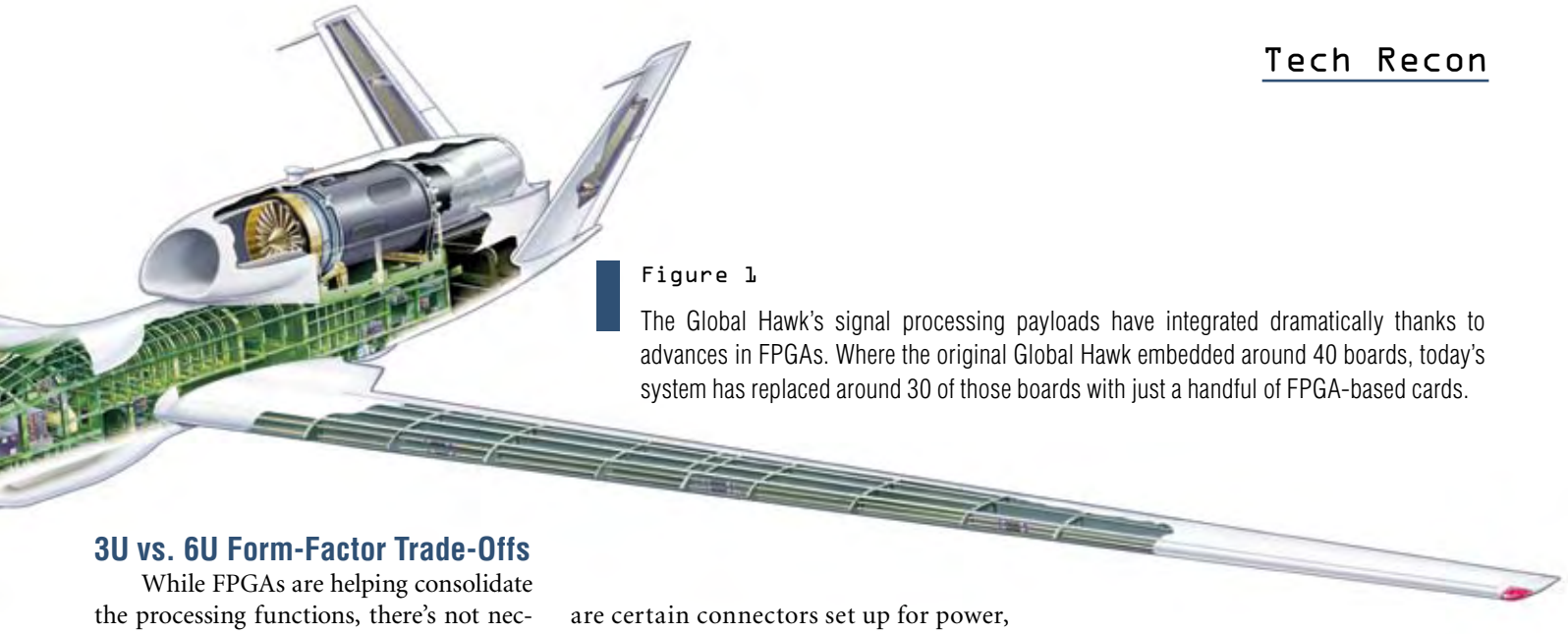

Figure 1

The Global Hawk's signal processing payloads have integrated dramatically thanks to advances in FPGAs. Where the original Global Hawk embedded around 40 boards, today's system has replaced around 30 of those boards with just a handful of FPGA-based cards.

3U vs. 6U Form-Factor Trade-Offs

While FPGAs are helping consolidate the processing functions, there's not necessarily a related shift happening in the size of boards best suited in complex UAVs like the Global Hawk. While many UAV platform designers are considering a move from 6U boards to 3U boards, 3U isn't always the best direction. Cooling is not the main issue here. For conduction-cooling, experts say, 3U is much better. It's easier to cool 3U than 6U when you're doing conduction-cooling because the chips are closer to the edge of the board, allowing heat to dissipate against the wedgelocks. In contrast, for air-cooling—most often used in UAVs aloft—3U and 6U rank about the same, with 6U having a slight advantage with its greater surface area.

The main reason 6U has an advantage is volume. "For applications such as UAVs that are calling for as much processing power as possible into a certain volume—airflow, heat dissipation and power being constant—I guarantee that 6U is a better choice than 3U," says Mercury's Jadon. The problem is volume and dimensions. If you compare three 6U boards as a system and compare the volume it takes up with the same volume comprised of 3U boards, it's impossible to get the same total volume that's possible with 6U.

A related issue is the matter of I/O. Even as FPGAs have enabled system designers to shrink down the number of boards in a UAV, there's a lot I/O that hasn't gone away. There's a variety of 1553, RS-422 and RS-232 I/O onboard the Global Hawk, for example, that ends up having to get packed on a smaller set of boards. Here again, 6U boards provide more front panel I/O stuff to accommodate all that. 3U is also a problem on the backplane connectors. There are certain connectors set up for power, certain ones for fabric buses and the rest of it is available for I/O. Two 3U boards compared to one 6U card in this case means a lot more connector space left over for I/O.

Stove-Pipe Fragmentation

In the development of new UAV payloads, one of the problems the defense industry faces is its lengthy acquisition and development cycle. Because they're non-traditional, UAVs don't fit neatly into that cycle. They usually get developed and deployed very quickly, which is why their payload and avionics subsystems get so stove-piped and fragmented. In payload development, the trend now is toward developing payloads very quickly using standard building blocks. And that's why you're seeing non-traditional payload houses come out.

According to Mercury's Lathrop, a good analogy is comparing the UAV industry in the U.S. today to the jet aircraft industry in the 1950s. Just as

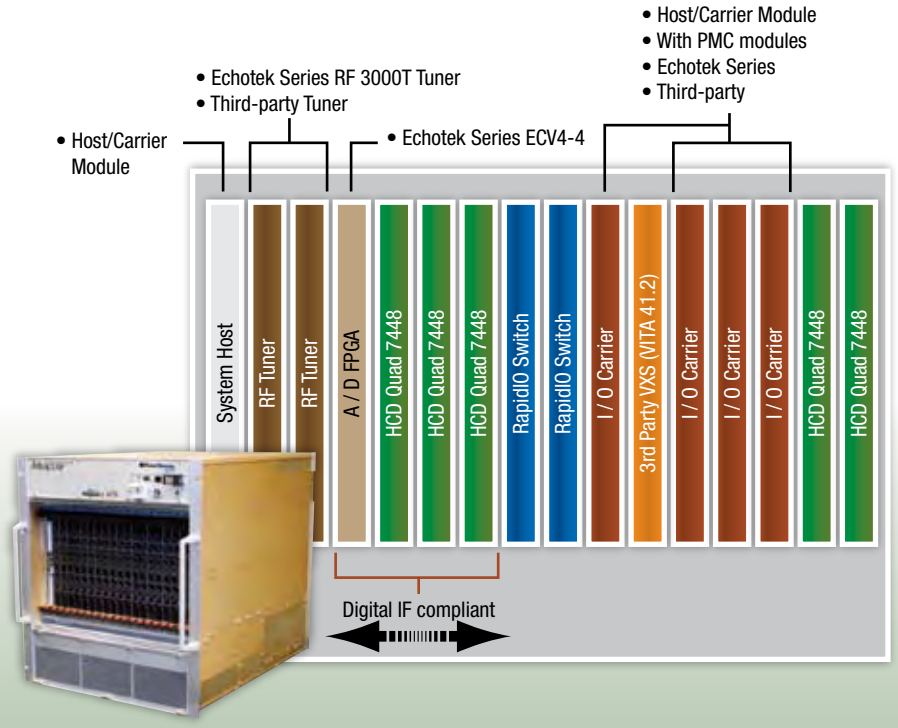

Figure 2

Exemplifying the idea of a pre-integrated system is Mercury's PowerStream 6100 box. It's designed for multi-INT and multi-mission computing in next-generation UAVs.

back then, fairly new technology has evolved to where it gets widely used, but is extremely non-standard. "One of the problems we have right now is that all the UAVs flying have been designed in extreme stove-pipes," says Lathrop. "The issue is that the diversity of needs and requirements and the diversity of ways to use a technology to solve those problems gives you a large number of solutions. As a result the standards get pushed down to a level that's very low. At one point the standards are down to basic IEEE standards, now they've moved up to where—more and more—you're seeing board-level standards."

ments on how they acquire the UAVs. For its part, the Air Force is trying to be the executive agent in those efforts, and the Army and the Navy are fighting that. In the end, Congress will have to push to eliminate the duplication of effort and resources that's happening in UAV development. Once those initiatives set in, it's expected that the UAV industry will "gel" a lot like the tactical aviation industry did in the 1960s.

For its part, Mercury has attempted to get ahead of the standards issue by putting together platform-level systems that are applicable to wide variety

Figure 3

The Continuous Look Attack Management for Predator (CLAMP) Program intends to develop and transition advanced sensor exploitation capabilities to the Long-Endurance Predator UAV. As the Predator UAV flies and collects data over a designated area for hours at a time, the multi-look, multi-sensor nature of its mission can be fully exploited.

The lack of standardized payloads has become such a problem that the Government Accountability Office (GAO) issued a report to Congress citing the matter. Congress is expected to soon mandate to the Services that they standardize on a number of require-

of UAV implementations. The argument is that the more components that come pre-integrated, the more finely integrated a system is when it's delivered for final integration into a UAV aircraft or payload, the better they can control their costs, risk and schedule. An example is the PowerStream 6100 box designed for multi-INT and multi-mission computing in next-generation UAVs (Figure 2).

Along similar lines, Mercury has proposed a concept for several years to have standardized central processing packages called ARIES be used across a range of UAV payloads. The idea was that since payloads themselves tend to be developed in a stove-pipe manor—there's a lot of redundancy. If a UAV carries three payloads, for example, it's probably carrying excess processing capability and a lot of other things that could be in common.

Last May, the Air Force Research Lab (AFRL) at Wright-Patterson Air Force Base came around to the concept, and selected Mercury Computer Systems to provide computer hardware and services for the Continuous Look Attack Management for Predator (CLAMP) Program. The goal of CLAMP is to develop and transition advanced sensor exploitation capabilities to the Long-Endurance Predator UAV.

CLAMP was the first U.S. Air Force program to undertake Mercury's ARIES (Airborne Reconnaissance Image Exploitation System) concept, in which airborne multi-sensor platforms will use stored sensor data for comparative purposes. ARIES is an adjunct processor that is designed to facilitate the migration of ground-based algorithms to the platform, adjacent to the sensor and with direct access to original sensor data, so that image exploitation can occur in real time.

As the Predator UAV (Figure 3) flies and collects data over a designated area for hours at a time, the multi-look, multi-sensor nature of its mission can be fully exploited. By enabling the UAV to store, retrieve and process sensor data over a long period of time, warfighters will be able to detect changes in tactical conditions and allow them to pinpoint attacks or avoid dangerous situations.

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Bus	AT Expansion Bus			✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI Universal Expansion Bus	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	
	PCI Bus Masters	4	4	4	4	4	4	4	4	4	4		4	
	APIC (add'l PCI interrupts)	9	9	9	9	9	9	9	9	9	9			
CPU and BIOS	CPU Max Clock Rate (MHz)	1400	1400	1400	1400	400	650	400	650	400	650	333	333	333
	L2 Cache	2MB	2MB	2MB	2MB	256k	256k	256k	256k	256k	256k	16K	16k	16k
	Intel SpeedStep Technology	✓	✓	✓	✓									
	ACPI Power Mgmt	2.0	2.0	2.0	2.0	1.0	1.0	1.0	1.0	1.0	1.0			
	Max Onboard DRAM (MB)	512	512	512	512	512	512	512	512	512	512	256	256	256
	RTD Enhanced Flash BIOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Nonvolatile Configuration	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Quick Boot Option Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	USB Boot	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
Peripherals	Watchdog Timer & RTC	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	IDE and Floppy Controllers	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	ATA/IDE Disk Socket, 32 DIP	1	1	1	1	1	1	1	1	1	1	1	1	1
	Audio	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
	Digital Video	LVDS	LVDS	LVDS	LVDS			TTL	TTL	LVDS	LVDS	TTL	TTL	
	Analog Video	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	
	AT Keyboard/Utility Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PS/2 Mouse	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	USB Mouse/Keyboard	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
I/O	RS-232/422/485 Ports	2	1	2	1	2	2	2	2	2	2	2	2	2
	USB 2.0 Ports	2	4	2	4									
	USB Ports					2	2	2	2	2	2	2	2	1
	10/100Base-T Ethernet	1		1		1	1	1	1	1	1	1	1	
	ECP Parallel Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	aDIO(Advanced Digital I/O)	18	18	18	18	18	18	18	18	18	18	18	18	18
	multiPort(aDIO, ECP, FDC)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SW	ROM-DOS Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	DOS, Windows, Linux	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

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Bus	AT Expansion Bus	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI Expansion Bus Master	✓	✓				✓							✓	✓
	McBSP Serial Ports	✓	✓				✓								
Analog Input	Single-Ended Inputs	16	16	16	16	16	16								
	Differential Inputs	8	8		8	8	8								
	Max Throughput (kHz)	1250	1250	40	500	100	1250								
	Max Resolution (bits)	12	12	12	12	16	12								
	Input Ranges/Gains	3/7	3/7	3/1	3/4	1/4	3/6								
	Autonomous SmartCal	✓	✓												
	Data Marker Inputs	3	3		3		3								
Conversions	Channel-Gain Table	8k	8k		8k	8k	8k								
	Scan/Burst/Multi-Burst	✓	✓		✓	✓	✓								
	A/D FIFO Buffer	8k	8k		8k	8k	8k								
	Sample Counter	✓	✓		✓	✓	✓								
	DMA or PCI Bus Master	✓	✓		✓	✓	✓	✓						✓	
	SyncBus	✓	✓				✓								
Digital I/O	Total Digital I/O	16	16	16	16	16	16	16	48	18/9	32	64	32	48	48
	Bit Programmable I/O	8	8		8	8	8	8	24	6/0				48	✓‡
	Advanced Interrupts	2	2		2	2	2	2	2					2	
	Input FIFO Buffer	8k	8k		8k	8k	8k							4M	8M
	Opto-Isolated Inputs										16	48	16		
	Opto-Isolated Outputs										16	16			
	User Timer/Counters	3	3	3	2	3	3	3	3	3				10	6
	External Trigger	✓	✓		✓	✓	✓	✓	✓					✓	
	Incr. Encoder/PWM									3/9					✓‡
	Relay Outputs												16		
Analog Out	Analog Outputs	2	2		2	2	2	4							
	Max Throughput (kHz)	200	200		200	100	200	200							
	Resolution (bits)	12	12		12	16	12	12							
	Output Ranges	4	4		3	1	4	4							
	D/A FIFO Buffer	8k	8k				8k	8k							

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Navy and Army Share Fire Scout Design

One UAV that boasts some success in sharing commonality between designs is the Fire Scout Vertical Takeoff and Landing Tactical Unmanned Aerial Vehicle (VTUAV). Although Fire Scout isn't technically a Joint Army/Navy program, the two branches are cooperating closely on it. An Army Lt. Col is embedded in the Navy program office (PMA). The Army has selected Fire Scout as its Class IV UAV for its Future Combat Systems program. For the Army Fire Scout, Northrop Grumman provides just the air vehicle for Boeing and SAIC—the Lead System Integrators for FCS—while Boeing does the avionics, including a different control system than the Navy version and a different datalink.

The Navy Fire Scout, much further along in its development, achieved first flight in January 2006. It was a groundbreaking system because it marked the first time a UAV performed vertical landings on a moving ship without a pilot controlling the aircraft (Figure 4). While an air vehicle landing on a fixed-site need only orient its landing path into the wind, landing on a ship requires the UAV to make corrections based on the relative motion of the ship. On top of all that throw in the unpredictable nature of a flight deck at sea—the pitching, rolling and heaving of the deck—and the problem become even more of a challenge.

All that complexity required a level of embedded computing power beyond that of any previous UAV. Northrop Grumman is in the process of developing the second-generation Fire Scout. Embedded computers and the payload interface unit aboard the MQ-8B are 3U CompactPCI boards supplied by GE Fanuc Embedded Systems. Offering size, weight and power advantages compared to 6U VME, 3U CompactPCI has become a popular choice for UAV designs. Also on the air vehicle are three Rockwell ARC-210 Radios, with a growth path that accommodates substituting those for JTRS Radios when they become available. Rounding out the onboard avionics are Raytheon's Tactical Control System (TCS) and BAE Systems' IFF (Identification Friend or Foe) system. The Unmanned Combat Automatic Recovery System, residing on the ship, is supplied by Sierra Nevada Corp. ▮▮

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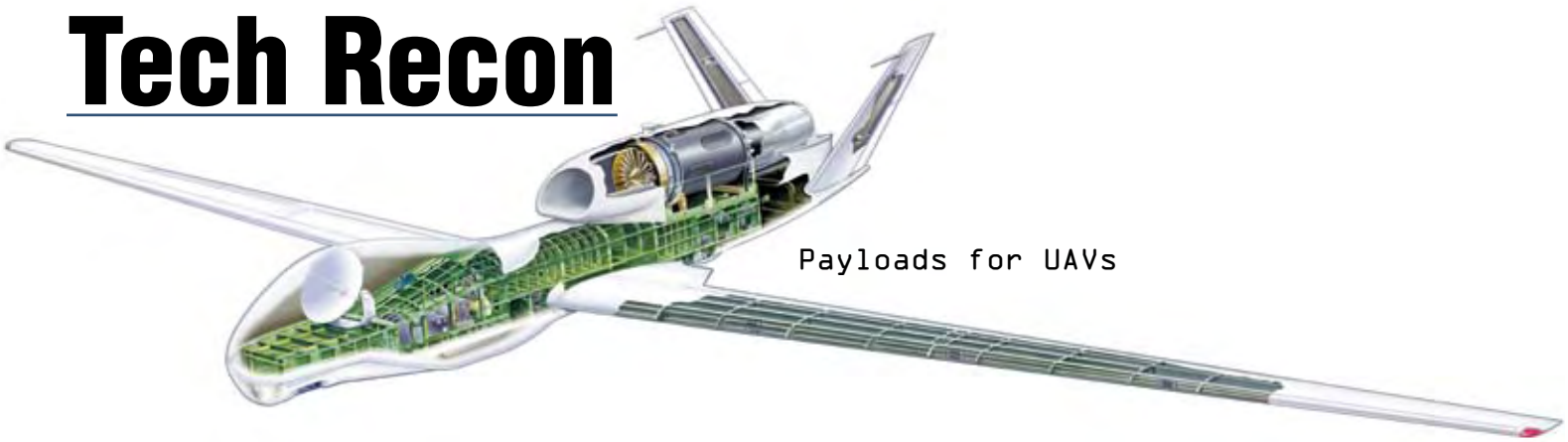
Figure 4

Embedded computers and the payload interface unit aboard the MQ-8B Fire Scout are 3U CompactPCI boards supplied by GE Fanuc Embedded Systems. Offering size, weight and power advantages compared to 6U VME, 3U CompactPCI has become a popular choice for many UAV designs. Shown here is the earlier version of Fire Scout as it makes its first autonomous landing on a moving aircraft carrier.

Tech Recon



Payloads for UAVs

Bandwidth Drives Sensor Net and Image Processing UAV Payload Designs

Sensor networks aboard UAVs are leveraging the benefits of packet-based communication. Meanwhile, image processing payloads are taking a turn toward small, embedded form-factors.

Jeff Child
Editor-in-Chief

As UAVs bulk up their sensor counts and processing payloads, the pressure is on to keep the data that's acquired and processed moving inside the system between nodes. That's driving the sensor management networks and image processing subsystems to embrace technologies that increase bandwidth and keep the data flowing. Also critical is the format of the data as the military transitions to a fully IP-based network-centric capability and all the advantages that entails.

The current version of the Global Hawk (Figure 1) that's flying now includes a Sensor Management Unit (SMU). The SMU provides a common interface between the sensor payloads and the rest of the aircraft systems. This enables sensor payloads to be easily redefined and changed without impacting the Operational Flight Program (OFP) and other subsystems in the aircraft.

Figure 1

Based on a hybrid 6U VMEbus and CompactPCI architecture, the Sensor Management Unit (SMU) is aboard the Global Hawk UAV. The SME provides a common interface between the sensor payloads and the rest of the aircraft systems. As a result, sensor payloads can be easily redefined and changed without impacting other subsystems.

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The SMU subsystem incorporates enhanced DSP capability, a solid-state hard drive and Fibre Channel data communications that interconnect the advanced sensor suite with the satellite and ground communications systems. The unit also interfaces with the existing dual-redundant Integrated Mission Management Computer. The SMU's 1 Gbyte/s Ethernet network provides communications redundancy and enables a remote operator to select onboard sensor data. For another twist on communications issues related to UAVs, see the sidebar "For UAV Comms: It's All About the Data" in this story.

Based on a hybrid 6U VMEbus and a CompactPCI rugged open-systems architecture, the first-generation SMU that's flying in the Global Hawk is packet-based. According to Val Zarov, program manager at Curtiss-Wright Controls Embedded Computing, the second-generation SMU, while also packet-based, goes further by tying its buses together with a fabric interconnect. Zarov says the SMU's architecture is designed such that upgrades can be made to interconnect switch technology without having to requalify the software, or redo the software from scratch. Curtiss-Wright makes both SMU and Integrated Mission Management Computer (flight control) systems aboard the Global Hawk.

Road to a Global IPv6 Network

Because the SMU packetizes the data that moves from system to system or within the system, all the systems it connects to can be tied together with a fabric such as switched Gbit Ethernet. And because it's Internet Protocol (IP)-based, the subsystem blocks can be virtually linked to each other onboard the UAV as well as system on blocks anywhere in the world. The ultimate goal is to leverage the advantages of IPv6. With IPv6, a centralized router is no longer needed, and organizations like the U.S. Military can have a huge network that's spread around the world, without a need for different subnets.

Being networked-based makes the SMU platform very generic from the perspective of software. Hardware upgrades to the unit to support higher-speed sensors have no impact on the software. The packetized data can also link over the myriad variety of I/O aboard the Global Hawk. Whether it's Fibre Channel, Gbit Ethernet, MIL-STD-1553 or even RS-422, if the data is moved in a packetized form it doesn't really matter what the physical link is.

Much of that slower legacy I/O could move to faster, more easy to work with protocols, by taking advantage of some other interfaces that are now standard in a commercial environment—such as USB or Firewire. So far, designers at

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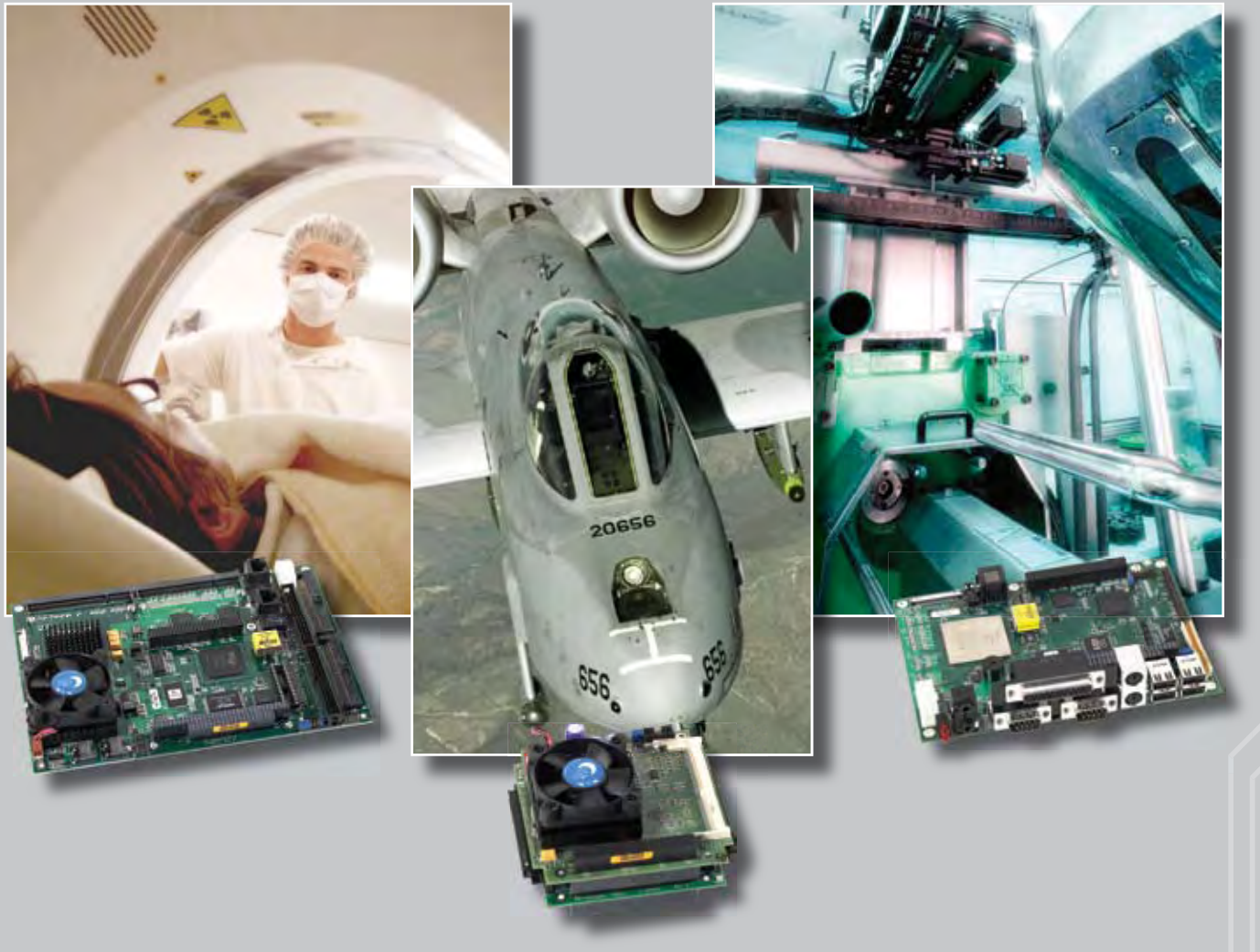

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For UAV Comms: It's All About the Data

UAVs serve increasingly strategic roles in a broad range of missions, including military reconnaissance, border patrol and search-and-rescue missions. A successful UAV mission requires both impressive autonomy and reliable ground-control, along with real-time data exchange both on the UAV itself and the ground control stations (GCSs). The variety of missions, along with the need for multiple airborne and ground systems to receive and process data from different sources, demands a flexible architecture and fast data access.

These characteristics demand a data-driven architecture that can respond to changes in control and mission parameters without undergoing reconfiguration. The design and implementation of structures for data creating, processing and transfer are critical for producing a UAV that can meet the array of intended uses.

Insitu has adopted a data architecture based on the Object Management Group (OMG) Data Distribution Service standard for publish-subscribe communications for real-time and embedded systems. Its unique publish-subscribe architecture lets instruments and processing nodes post results to a shared memory area, and enables data consumers on the network to subscribe to data by accessing the designated shared memory. All data writes and reads occur at a high level of performance and with reliable response parameters.

The Data Distribution Service also incorporates a high level of control of Quality of Service parameters, including reliability, bandwidth, delivery deadlines and resource limits. This ability provides all components of the UAV system with the ability to prioritize based on the data needs of various system components.

Insitu uses the Real-Time Innovations (RTI) implementation of the Data Distribution Service in multiple portions of its UAV platforms, such as on the UAV itself, in the GCSs, and in future air-to-ground communications systems. The company's next-generation ScanEagle (see Figure) is an example of a UAV using this technology. On the UAV airframe, the Data Distribution Service connects the flight computers, sensors and onboard application computers. Within the GCS, the Data Distribution Service connects the systems that decode data feeds, analyze the UAV's situation and interface to the operator control.

Using the Data Distribution Service also lets UAV developers such as Institu create innovative data architectures that fully exploit the capabilities of the hardware and programming. All too often a platform is over-engineered, in that the software is not able to take full advantage of its design envelope. As Insitu demonstrates with its UAV platforms, that doesn't have to be the case. Thanks to real-time data availability using the Data Distribution Service, software engineers can bring performance and flexibility characteristics closer to the capabilities that the hardware can provide.

Figure
Institu uses RTI implementation of the DDS in platforms such as Institu's next-generation ScanEagle UAV. DDS connects the UAV's flight computers, sensors and onboard application computers.

Real-Time Innovations
Santa Clara, CA.
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[www.rti.com].

Global Hawk prime contractor Northrop Grumman are avoiding those consumer high-speed interfaces because of the risk that they could disappear from the market over the long term.

Powering Down on the Tarmac

According to Curtiss-Wright's Zarov, the second-generation SMU, although providing triple the capability of its predecessor, does draw double the power compared to the older version. Meanwhile, the subsystems the SMU links to are likewise drawing more power. That added power means more heat dissipation. And while that heat can be expelled via air-cooling when the Global Hawk is aloft, when the UAV is sitting on the tarmac the problem can be acute.

With that in mind, Curtiss-Wright has written its Board Support Package for the SMU's boards to accommodate power management features. That means that, while on the tarmac, the box can be powered up without really running at full speed. The CPUs can go idle because there is typically no application being executed while the UAV is on the ground. The box can essentially be put to sleep—aside from some self-checking—until the higher application calls for it.

Image Processing Still a Dedicated Unit

Like the sensor networking aboard UAVs, image processing is another area where bandwidth is key. Aside from the Global Hawk, the image processing functionality aboard most UAVs is still in the "dedicated image processing element" era. Aside from spacious UAV airframes like the Global Hawk, most of the more tactical UAVs don't have enough processing power in their general-purpose computing core to take on image processing tasks.

"What we're seeing as a company is that because in general UAVs are getting smaller, therefore the electro-optic (EO) payloads are getting smaller," says Roger Joel of GE Fanuc Embedded Systems. "So there's a big drive for us to reduce the volume and power consumption of our electronics and put them into special format boards that can then be specifically located inside the envelope of the EO system itself."

GE Fanuc provides the electronics inside the EO system aboard the Sperwer UAV (Figure 2), the most common European UAV, built by Sagem Défense Sécurité, Paris France. GE Fanuc's board handles target detection and video tracking aboard the Sperwer. The Sperwer currently flying uses a relatively older product that's in a 3U VME format.

In keeping with that same trend, most of the EO payload manufacturers are pushing down the road of no separate electronics box, but rather one single unit

Figure 2

Built by Sagem, the Sperwer UAV is perhaps the most common European UAV. The Sperwer version now flying does its target detection and video tracking using a relatively older product that's in a 3U VME format.

Figure 3

Makers of Electro-Optic payloads for UAVs are trying to put all the required electronics within the EO unit itself. That's driving designers to solutions like GE Fanuc's ADEPT104. This PC/104-compatible card integrates an AXIS MultiComputer System Blade, Single Board Automatic Video Tracker, plus two RS170/CCIR analog video inputs and outputs, and serial and parallel digital video interfaces.

that basically bolts to the UAV. The idea is to house all of the necessary electronics, including all the image processing, target tracking and so forth, for that system into one unit. In order to get the required electronics into that volume envelope, system designers are looking toward smaller dedicated hardware in the small PC/104 form-factor or similar-sized non-standard form-factor.

An example along those lines is the ADEPT video tracker family of boards from GE Fanuc Embedded Systems, formerly the Octec Image Processing division of Radstone. The PC/104-compatible ADEPT104 (Figure 3) includes an AXIS MultiComputer System Blade, Single Board Automatic Video Tracker, comprehensive suite of detection and tracking algorithms, two RS170/CCIR analog video inputs and outputs, serial and parallel digital video interfaces accommodated by daughter boards, full graphics overlay capability and extended temperature range.

Onward Toward Tactical UAV Autonomy

GE Fanuc's Joel foresees three phases in the evolution of UAV capabilities, again referring mainly to tactical (smaller than Global Hawk) UAVs. "You could say that we've come to the end of what I'd call the first generation of UAVs—where the issue was getting it up in the air and getting it to stay there and then come back down when you wanted it too." In that first phase, the priority for the prime contractors was UAV flight and UAV safety. Those issues have been solved and matured.

With that in mind, the industry is now, according to Joel, in its second phase where the goal is to provide more processing onboard the UAV and to add more sophistication into the image processing. Tactical UAVs are starting to do things like some level of target classification and those sorts of activities," says Joel. "And potentially processing some of the imagery so that it's not necessary to transmit everything continuously." That reduces the bandwidth requirements for sending info to the ground.

After that, at some point in the future in Joel's view, is a move to phase three, which means moving into the realm of total autonomy where the UAV is able to go off and activate itself, look for targets, find them and then decide what to do with them without reference to the ground. "Realistically we're probably 10 years from that point," says Joel. "In the next 5 to 7 years the focus will be on adding more image processing capability into UAVs." ▮▮

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System Development

Precision Time for Mil Networks

IEEE 1588 Keeps Military Packet Networks in Synch

Demand for very precise timekeeping technology is on the rise in military applications. IEEE 1588 delivers a solution that's efficient in its use of space and weight.

Paul Skoog, Product Marketing Manager
Symmetricom

For decades, while many of the military's electronic systems have migrated to IP networks as the preferred way to exchange data, one key system has not: the distribution of timekeeping in applications that require very precise synchronization. Those applications include everything from time correlation of telemetry data to range finding in missile launches.

Since the 1950s, technology based on the IRIG (Inter-Range Instrumentation Group) standard has served many "sync sensitive" applications well. In IRIG, systems acquire synchronization from a time source via an analog waveform over a dedicated wire. The source may be a GPS receiver or a clock connected to a GPS receiver. All systems connected to the IRIG time code source stay in sync within the limits of the IRIG standard.

Two Drawbacks for IRIG

IRIG, however, poses two drawbacks. The first is precision. At 1 to 10 microseconds, IRIG is still adequate for many applications—but not for newer applications that require precise time references with synchronization over a packet-based network. Examples include sensor netting and integration aboard submarines (Figure 1) and shipboard radar systems. Sub-microsecond timing is also becoming more important in traditional applications like correlating the data acquired from test vehicles—given today's higher velocities and greater volumes of data.

The second IRIG drawback is poor efficiency—in cost, space and weight. Not only does IRIG require a dedicated coaxial cable network solely to distribute synchronization, that network's hierarchal topology often duplicates the Ethernet-based data network. All that extra copper increases weight, takes up space, and adds complexity that can impair mission performance especially in contained environments like ships.

Efficient data exchange among systems is, however, a key benefit of IP networks. So why not distribute synchronization via Ethernet? Synchronization packets distributed over an existing IP network would eliminate the need for a duplicate network solely for timing. Ethernet's drawback, however, is that it is non-deterministic, in other words packet transit times can vary randomly, which diminishes accurate time transfer. That is the reason for a newer synchronization standard: IEEE 1588. This standard can achieve highly accurate synchronization over Ethernet—down to 100 ns in a LAN deployment—even with normal network traffic coexisting on the same network.

Obstacles to Accurate Network Synchronization

Here's how IEEE 1588 works and how network designers can use it to overcome the obstacles inherent in synchronizing events over a network. There are two key obstacles inherent to network synchronization: oscillator drift and variable time-transfer latency. Oscillators in electronic equipment maintain the frequency used by counters to maintain the time. No matter what method of time distribution is employed, an oscillator will drift over time—becoming out-of-sync with other oscillators—unless it is periodically adjusted from an accurate external timing source. Oscillator drift can be mitigated

by using more accurate (higher quality) oscillators and by more frequent adjustments from an accurate external source such as the GPS satellite system. However, installing a high-quality oscillator everywhere an accurate time or frequency source is needed is expensive and impractical. The same is true for placing a GPS receiver at those locations.

Time transfer latency is the amount of time it takes (the delay) for packets containing time stamps to reach the remote clock (a slave) from the accurate time source (a master). These time stamps contain the information to ultimately adjust the remote clock's oscillator—mitigate drift in other words. The longer the path to reach the remote clock, the greater the chance the packet will be delayed by a network element such as switch, and the greater the difference between the time stamp and the time the slave actually receives the time stamp. Furthermore, the amount of delay varies from packet to packet—a condition called packet delay variation (PDV). Packet delay will vary when going from master to slave as well as when going from slave to master—a condition called asymmetric path latency.

Both conditions are why NTP (Network Time Protocol) has not replaced IRIG as a way to distribute time in sync-sensitive applications. NTP is widely used on IP networks in military and commercial environments. NTP time servers provide accurate time stamp packets to clients, which read the time and adjust their clocks accordingly. NTP time servers are widely available on the Internet and many computer operating systems have NTP clients built in. However, a time client using NTP can generally only synchronize to within the 0.5 to 2 ms of the time server over a LAN.

Figure 1

At 1 to 10 microseconds, the IRIG standard isn't precise enough for newer applications that require precise time references with synchronization like, for example, the sensor netting aboard submarines. Shown here, the USS Virginia (SSH-774) is designed to accommodate various modular payload options including intelligence, surveillance, reconnaissance and target acquisition; undersea communications and sensor network systems; UAVs; and unmanned underwater vehicles (UUVs) and more.

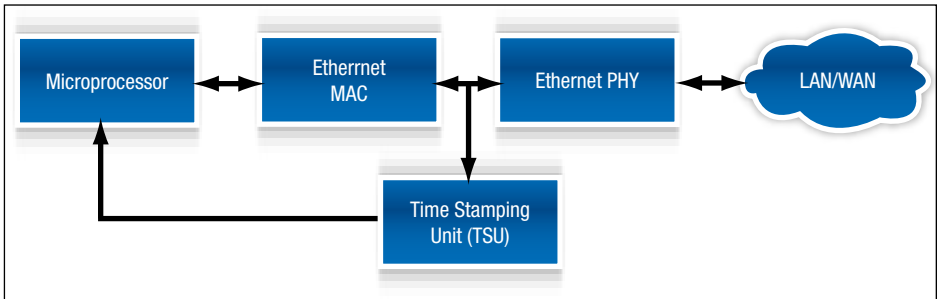

Figure 2

Hardware time stamping reduces effects from softwares's non-deterministic latencies.

How IEEE 1588 Works

IEEE 1588 defines PTP (Precision Time Protocol) that builds on many of the principles of NTP but takes special measures to mitigate PDV. The three key measures are hardware time stamping, PTP sync messages and PTP-enabled Ethernet switches called boundary clocks and transparent clocks.

Much of the PDV associated with NTP results from using software to issue time stamps. The time stamp unit (TSU) is a software program that is called by the time server's operating system (also a program). This introduces non-deterministic latencies generated by:

- CPU context switching
- Saving and restoring states
- Flushing caches around the invocation of the interrupt handler
- Queuing as the packet makes its way through the protocol layers to the application and back to the network

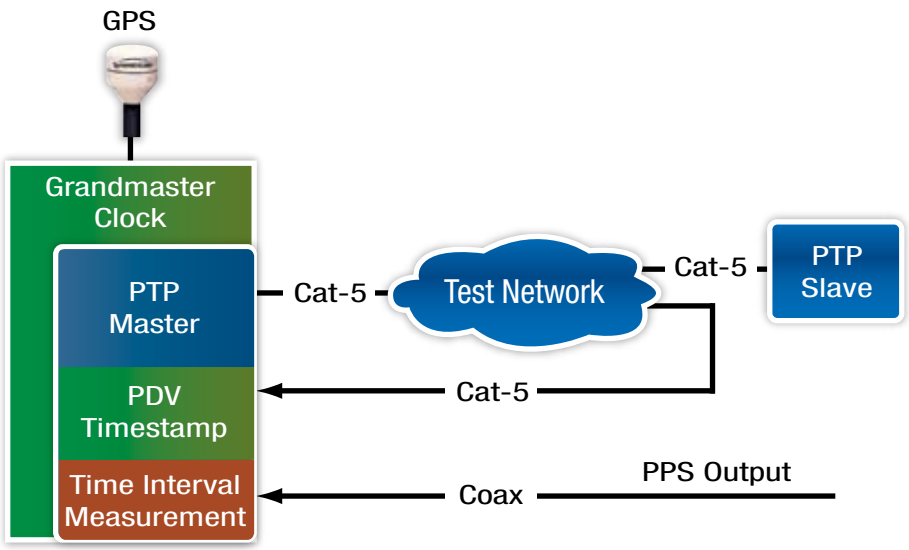

Figure 3

A grandmaster clock with built-in PDV and time interval measurement allows network designers to evaluate the performance of alternative network topologies.

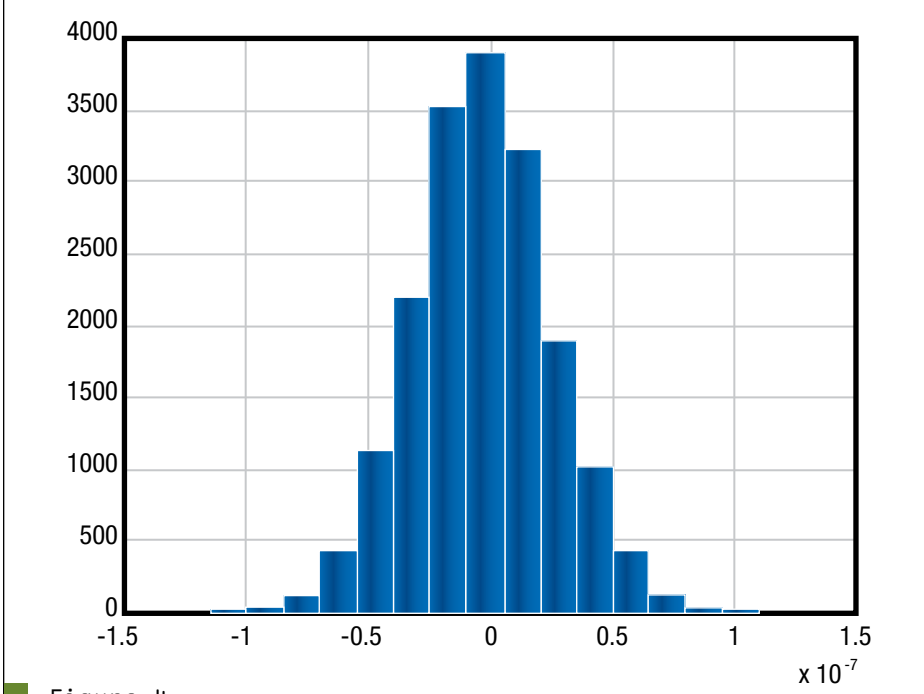

Figure 4

Plotting a slave PPS relative to the master PSS as a histogram shows the statistical nature of slave synchronization and the intervening network, best described by mean and standard deviation.

PTP avoids these latencies by implementing the TSU in hardware between the Ethernet Media Access Control (MAC) and the Ethernet PHY transceiver. The TSU sniffs both inbound and outbound traffic and records a time stamp when the leading bits of an IEEE 1588 packet are identified, precisely marking the arrival or departure of PTP time packets very close to the network port (Figure 2).

Hardware time stamping addresses software-based latencies but still leaves the problem of network-based latencies—which are addressed by PTP sync messages and PTP-enabled switches. PTP sync messages communicate between masters and slaves (i.e., devices whose internal oscillators get reset). They consist of:

- Sync Message: A message from the master clock containing time and other information.
- FollowUp Message: A second message from the master clock that contains the exact time the Sync Message left the master clock.
- DelayReq Message: A request from the slave to the master to measure delay.
- DelayResp Message: A response from the master to the slave with the measured arrival time of the DelayReq packets at the master.

To further mitigate operating system latency as well as network latency, PTP employs message exchanges as described in Table 1.

Multicasting and Switches

By default, masters multicast PTP packets every two seconds. Periodically (about every 30 seconds) slaves send a DelayReq message to the master. PTP also employs special switches called boundary clocks and transparent clocks. A boundary clock is a multi-port switch with a very accurate internal clock. The switch acts as a time transfer standard between the upstream master and downstream slaves. In other words, besides moving data traffic between devices, it also is an intermediate clock used to transfer time.

One port is a PTP slave to a master clock, and the other ports are masters to downstream slave clocks. There may also be other regular switches downstream between the boundary clock and the slaves. The boundary clock receives PTP packets hardware time stamped by its master. It also hardware time stamps the PTP packets it sends to slaves. Because boundary clocks do not forward PTP packets, PTP packets do not suffer latency effects due to forwarding or queuing within the switch.

Deploying boundary clocks at existing points of network traffic congestion is therefore a good way to reduce latency—since PTP packets would not have to compete with other packets going through the switch.

A transparent clock is also a multiport switch with a very precise internal clock. Unlike the boundary clock, however, it does forward PTP packets but adjusts the packet time stamps for the switch-induced delay. Specifically, it measures the time the Sync and Delay request messages reside in the switch, then modifies the time stamps within the DelayResp and FollowUp messages to account for those delays. The result is improved sync between slave and master clocks.

To calculate one-way delay …	To calculate roundtrip delay …
1. Based on its local clock, master sends a Sync Message to slave	1. Slave sends a DelayReq to master with a time stamp of its departure
2. Master's TSU marks the exact time Sync Message is sent	2. Master issues a DelayResp to slave with a time stamp of when it received DelayReq
3. Master sends a FollowUp Message to slave with exact time Sync Message was sent	3. Slave combines this difference with one-way delay (column 1) to calculate round-trip offset
4. Slave compares Sync Message arrival to departure time provided in FollowUp	4. Slave uses roundtrip offset to adjust for latency when referencing master's time stamps
5. Slave calculates one-way delay	

Table 1

Messages between master and slave clocks help handle time transfer latencies. To find one-way delay (master to slave), column 1 applies. To find round-trip delay, column 2 applies. Knowing the round-trip delay enables the slave to compensate for latency when referencing time from the master.

Optimizing PTP Deployments

PTP's features lend themselves to several strategies that can ensure the accuracy of the synchronization delivered over a packet network. These include:

- Select the right grandmaster
- Characterize the network
- Design the right network topology

Because it is the ultimate source of time on the network, accuracy and load capacity are prime considerations in selecting a master clock (also called the grandmaster). A grandmaster can typically time stamp PTP packets with an accuracy of 30 ns-rms to UTC (Coordinated Universal Time). Operating at 100Base-T line speed with deep time stamp packet buffers, a grandmaster can support hundreds or thousands of PTP clients.

In addition to high precision and high capacity, a grandmaster may also contain features that help network designers characterize the network and optimize topologies. These features include time interval and PDV measurement capabilities. Most PTP slaves output a 1PPS (pulse per second) signal that—when provided back to a grandmaster that has time interval measurement capabilities—can measure the accuracy between master and slave. Similarly, attaching the grandmaster's PDV input port to the far side of the network under test can measure the amount of PDV present (Figure 3).

Plotting the time interval measurement—difference between slave 1PPS edge relative to the master 1PPS edge—as a histogram reveals the quality of the slave synchronization in terms of mean and standard deviation (Figure 4). Plotting PDV reveals the quality of the network in a similar way.

Based on these measurements, a network designer may decide to change the network topology—for example, making the network "flatter" by deploying masters closer to the slaves, deploying more masters (attached directly to GPS), or reducing the number of switches or hubs between masters and slaves. Designers can also replace standard switches with boundary clocks or transparent clocks at those points where PTP packets would otherwise compete with data packets for an output port.

Ultimately, the need for accuracy is determined by the application. If characterization studies find that slave accuracy mean and standard deviation fall within acceptable limits, then further mitigation steps may not be needed. What is important is that, with IEEE 1588's PTP, it is now possible to distribute highly precise synchronization to sync-sensitive applications and still realize the cost and flexibility benefits of IP-based packet networks. ■■

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MIL-STD-1553 Keeps Aloft Even as Alternatives Emerge

When data integrity and low latency are the priorities, MIL-STD-1553 still remains the military interface of choice. Fibre Channel, Ethernet and Extended 1553 top the list of possible upward migration paths from 1553.

Jeff Child
Editor-in-Chief

With over three decades now under its belt, the venerable MIL-STD-1553 bus still ranks as the dominant, internationally accepted data bus standard for many military platforms. While it's fundamentally an aircraft bus, all manner of craft such as tanks, ships, missiles, satellites and even the International Space Station, make use of 1553. Air Force, Navy, Army and space agencies of nations around the world have adopted 1553.

All those 1553 users continue to be well fed by an established infrastructure of subsystem suppliers. In fact, a key part of 1553's ecosystem is its acceptance into other bus and interconnect realms. Even consolidation caused by mergers and acquisitions in the embedded board business haven't seriously hurt the range of product choices available. As the Product Roundup on the following pages shows, products with 1553 interfaces exist in myriad board form-factors including VME, CompactPCI, PMC, PrPMC, PC/104 and others.

The most recent activity on the 1553 standards front is Edgewater Computer Systems' flavor of 1553 called Extended 1553. Also known as MIL-STD 1553B Notice 5, the technology has previously been demonstrated in a number of developmental and simulation environments including the C-130, F-16 (Figure 1) and F-18. In December, Edgewater's E1553 technology was tested on a U.S. Navy A-3 jet aircraft operated by Raytheon at Raytheon's Flight Test Operations Center in Van Nuys, California. For the purposes of the test, E1553 was coupled onto the internal 1553 Navigation Bus of the A-3, which also hosted other legacy 1553 Line Replaceable Units (LRUs) communicating concurrently on the same bus. Raytheon verified that no bus errors were reported on the legacy 1553 equipment during the flight.

Boosting 1553's Bandwidth

Adding high-capacity networking across the existing 1553 bus without changing the legacy software or disrupting the legacy communications has implications. The rate monitor maintained a consistent connection of greater than 100 Mbits/s through the entire flight. In March 2006, the U.S. Air Force sponsored the revision to MIL-STD 1553B referred to as Notice 5, which is based, in large part, on Edgewater's development of E1553.

Figure 1

Last December Edgewater successfully demonstrated its Extended 1553, or E1553, data bus technology in a flight demonstration. Also known as MIL-STD 1553B Notice 5, the technology has previously been demonstrated in a number of developmental and simulation environments including the C-130, F-16 (shown) and F-18. This F-16 Fighting Falcon is taking off from a base in Iraq to perform a close-air-support mission for coalition ground forces. *(U.S. Air Force photo)*

For several years now much speculation has centered on what interconnect technology will take 1553's place. Fibre Channel looks to be a strong candidate, but signs of such migration have weakened in the past few years. Meanwhile, Ethernet is coming into the picture as perhaps a more attractive migration path up from 1553. An important strength of Ethernet is its standardized software infrastructure. For its part, MIL-STD-1553 has never had a standard software API, which has forced 1553 subsystem vendors to craft their own APIs. ▮▮

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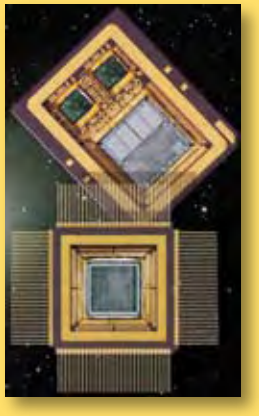
1553 Boards Roundup

Pair of 1553 Chips Ready for Rad-Hard Duty

The fact that the 1553 bus is popular in space-bound systems is testament to its reliability. Chips implementing the bus need to meet the rigorous space qualification standards to succeed in such applications. Meeting just those needs, Aeroflex Colorado Springs provides the MIL-STD-1553 RadHard SUMMIT family, available to SMDs, QML Q and V for space applications. The chip is



offered in two versions: the UT69151 SUMMIT E and the UT69151 SUMMIT LXE/DXE. The SUMMIT E features comprehensive BC, RT and MT, and is fully compliant with MIL-STD-1553B Notice II RT. Simultaneous RT/MT is provided along with autonomous operation in all three modes. Packaged in an 85-pin PGA and 84- or 132-lead flatpack, the UT69151 SUMMIT E is available qualified to SMD 5962-92118, QML Q & V and RadHard to 3.0E5 rads (Si).

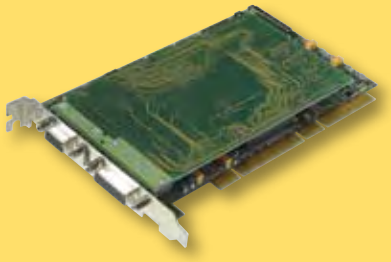
Meanwhile, the UT69151 SUMMIT LXE/DXE also offers comprehensive BC, RT and MT, but boasts integrated transceivers and offers a flexible power supply configuration. It supports -15V to 5V; -12V to 5V), or 5-volt-only. The device is available packaged with ceramic multichip module technology that is MIL-M-38510 compliant. Package styles include a 96-pin PGA and 100-lead flatpack. The UT69151 SUMMIT LXE/DXE is available qualified to SMD 5962-94663, QML Q and V and is RadHard to 3.0 E5 rads (Si) (DXE) and 1.0 E5 rads.

Aeroflex Colorado Springs
Colorado Springs, CO.
(719) 594-8000.
[www.aeroflex.com].

1533 Cards Marry PCI-X and XScale CPUs

Old it may be, but the MIL-STD-1553 bus standard remains a popular, reliable solution as a deterministic control interface technology. AIM-USA continues to support 1553 fans with its new pair of fourth-generation, PCI-X-compatible cards for test, simulation and monitoring applications. The APX1553-2 (shown) is a dual stream, dual redundant card while the APX1553-1 is a single stream, dual redundant card. Both are provided on a PCI-X-compatible, short-length card format. The APX1553 cards are available as Full Function, Single Function and Simulator-only versions, include an onboard IRIG-B time code generator/decoder, and can monitor/stimulate up to eight discrete I/O signals.

The new APX1553 cards offer unparalleled performance by using one or two 400 MHz XScale Processors for the BIUs (Bus Interface Units) and an additional 400 MHz Intel IOP80219 Application Support Processor.



Global memory from 1 to 4 Mbytes is provided plus 128 Mbytes of application support processor memory. An onboard IRIG-B time generator/decoder is included, having a sinusoidal output and free wheeling mode for time tag synchronization on the system level using one or more APX1553 cards. Both boards are able to stimulate/monitor eight general-purpose discrete I/O (GPIO) signals.

AIM-USA
Elkhorn, NE.
(866) AIM-1553.
[www.aim-online.com].

PMC Suits 1553 up for Space Applications

Airborne or battlefield ruggedness is one thing, but outfitting a board for use in space requires a whole other level of qualification. Exemplifying that trend, Aitech Defense Systems provides the S703, a MIL-STD-1553B I/O PMC—compliant with the PCI 2.1 interface and optimized for minimum traffic

on the host PCI bus. The card provides fast, high-speed access for dual redundant 1553B channel (BC/RT/MT) for low earth orbit (LEO) and Mars terrestrial applications, with an option for Geosynchronous Orbit (GEO) environments. Fully radiation qualification tested to well over 35K Rad (Si) (unshielded), the S703 is categorized as a single-function PCI device, with separate dedicated register sets accessible from the PCI bus to control each of the functional modules integrated on the card. And, with even a minor amount of spacecraft outer shell or mission computer enclosure shielding, the S703 can survive the radiation rigors of deep space.

The 1553B interface includes a space-rated DDC SpaceAce hybrid device, featuring a dual encoder/decoder, complete MIL-STD-1553B protocol, 32 or 64 kwords of shared RAM, memory management logic for all three modes (BC/RT/MT), a backplane hardwired or software RT address, and integrated built-in test capability. The 1553B channels can be specified as direct coupled or transformer coupled, with I/O available from the backplane. High-power components are cooled by an aluminum heatsink, which also adds to radiation shielding and higher radiation tolerance. Pricing for the S703 starts at $13,200.

Aitech Defense Systems
Chatsworth, CA.
(888) 248-3248.
[www.rugged.com].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1553 PMC Features Auto Message Transfer

Efficient message handling is a helpful feature in 1553 subsystems. Along those lines, Alphi Technology offers the PMC-1553-PLX, a single-wide PMC form-factor, which is based on the UTMC SUMMIT chip. Providing one or two dual redundant channels, the card provides system designers a versatile solution to multiplexed serial data bus design requirements. The PMC-1553-PLX board minimizes PMC host overhead with its automatic execution of message transfers, interrupt handling and generation of status information. In the Bus Controller mode, the PMC-1553-PLX implements a linked list

message scheme to provide the system with message chaining capability. In the Remote Terminal mode, time tagging and message history functions are available. The PMC-1553-PLX also allows multiple message processing, programmable automatic message delay, and automatic polling and retry.

Standard operating temperature for the board is 0 to +70°C, with an optional temperature range of -25° to +80°C. The board's humidity range is 5 to 90 percent and it operates at altitudes from 0 to 10,000 feet. Power consumption is 1.5W. Shock and vibration specs for the product are 0.5G RMS, 20-2000 Hz rand and 20 G, 11 ms, 0.5 sine. Mean time before failure is rated at 250,000 hours. Software support for the two products include a "C" Library Toolkit and driver support for many of the real-time OSs, such as Windows, NT, VxWorks and OS-9.

Alphi Technology
Tempe, AZ.
(480) 838 2428.
[www.alphitech.com].

PowerPC PrPMC Sports 1553 Interface

The OmniBus PMC is a MIL-STD-1553 to PMC interface combined with a PowerPC PrPMC, Serial I/O and avionics discretes. The product can be obtained with 1 or 2 dual redundant 1553 buses and in commercial or conduction-cooled versions. The PrPMC offers the user a monarch/non-monarch PrPMC with DMA, at the cost of just a MIL-STD-1553 interface. The PowerPC is provided as a user programmable device that when combined with the optional development kit, can control I/O, function as a system back-up controller and even record directly to user provided disk.

The OmniBus 1553 PMC can be a peripheral to a host processor system, or it can be operated as a stand-alone device using the PowerPC embedded processor. The MIL-STD-1553 channels are implemented as hardware modules external to the processor. This results in the user having full utilization of the processor while protocol operations are autonomously performed in hardware. The OmniBus architecture ensures all schedules will be maintained and all data will be received, on fully loaded 1553 databuses.

Transmit schedules, message structures and sequential monitor records are all stored in shared memory accessible by both the processor and the protocol hardware. A DMA mode is provided for efficiently transferring data from the onboard sequential monitor to the host processor. The OmniBus PMC is available for Windows, VxWorks, Integrity, Linux and other operating systems.

Ballard Technology
Everett, WA.
(425) 339-0281.
[www.ballardtech.com].

Switch Panel Multiplexes Sixteen 1553 Buses

When implementing avionics simulations or test scenarios, the chore of rewiring between different 1553 bus channels can be time consuming. Addressing that problem, Curtiss-Wright provides the MBX1553 Multiplex Bus Switch. The switch is designed to enhance virtually any MIL-STD-1553 system by providing a "virtual patch panel" housed in a 19-inch rack-mountable 1U chassis. This 16x16 crosspoint switch provides differential connections from 16 transformer-coupled Line Replaceable Unit (LRU) ports to 16

MIL-STD-1553 differential buses. The LRU units can be any MIL-STD1553 device: bus controller (BC), remote terminal (RT), or bus monitor (BM). Although the switch supports 16 non-redundant LRUs, it can also be used with dual (or more) redundant devices.

The MBX1553 switch provides 16 LRU ports via standard concentric twinax connectors on the front of the unit. The 16 bus port connections, which all use the same type of connectors, are available on the rear of the unit. Multiple switches may also be connected together if more LRU inputs or bus connections are desired. The MBX1553 switch configuration is controlled via an internal processor and associated RS-232 serial port. LRU ports may be selectively connected to (or disconnected from) a specified bus. The internal controller ensures that each LRU is not simultaneously connected to more than one bus. The MBX switch command set is thoroughly documented in the user's guide, allowing the user to provide control through a dumb terminal or to write separate communication software.

Curtiss-Wright Controls Embedded Computing
Leesburg, VA.
(703) 779-7800.
[www.cwcembedded.com].

1553 PCI-104 Card Supports IRIG-106 Chapter 10

PCI-104—which is basically PC/104-Plus sans ISA bus—is a popular form-factor for space-constrained rugged applications. Data Device Corp. has introduced a new PCI-104 card with up to four dual-redundant MIL-STD-1553 channels, five user-programmable digital discrete I/Os, selectable external or internal time-tag clock, and an IRIG-B time synchronization input. The new BU-65577C is a rugged card that can be used in both convection- and conduction-cooled applications. The PCI-104 and PC/104 Plus form-factors are commonly used in flight data recorders, displays and other avionics systems.

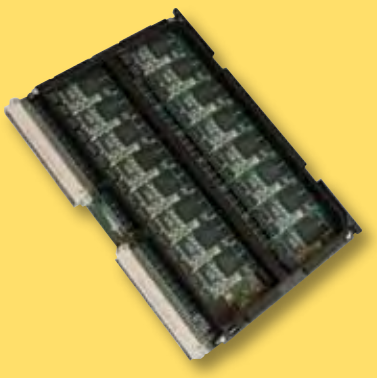
The BU-65577C card utilizes DDC's Extended Enhanced Mini-ACE (E2MA) Architecture. E2MA supports new standard features for each 1553 channel such as 2 Mbyte RAM with parity per channel, 48-bit/1 microsecond or 100 nanosecond time tag

and built-in self-test. Its intelligent hardware offload engine provides extremely low PCI bus and host CPU utilization while storing 1553 Monitor data in a convenient IRIG-106 Chapter 10 format. The high-level library functions abstract all register accesses and memory allocation so that no specific hardware knowledge is required. The BU-65577C series is now available.

Data Device Corp.
Bohemia, NY.
(631) 567-5600.
[www.ddc-web.com].

Conduction-Cooled VME Card Does Sixteen 1553 Channels

High channel count, onboard self test and loop back all rank high on the list of priorities when choosing a 1553 solution. Excalibur Systems addresses all those points with its latest card in its MIL-STD-1553 Px family. The EXC-1553ccVME/Px is a multi-channel (up to sixteen) MIL-STD-1553A/B interface board for conduction-cooled VME systems. The channels are fully independent, dual redundant, each of which can operate simultaneously as a Bus Controller and up to 32 Remote Terminals,



and also as a Triggerable Monitor. The card supports extensive error injection and detection capabilities, and an internal loop back, which requires no external cabling.

The card has an operating temperature range of -40° to +85°C and may optionally be ordered with conformal coating. It is supplied with C drivers, including source code and Merlin+ Windows software. The EXC-1553ccVME/Px is designed for rugged embedded applications, especially those requiring operation in a sealed, conduction-cooled, extended temperature environment.

Excalibur Systems
Elmont, NY.
(800) MIL-1553.
[www.mil-1553.com].

PMC Provides Interface for 10 Mbit/s 1553

The 10 Mbit/s flavor of MIL-STD-1553 boosts the venerable 1553 protocol up by an order of magnitude of bandwidth. The P-10SF from GE Fanuc Embedded Systems offers one or two channels of dual-redundant 10 Mbit 1553 Notice 2 protocol using RS-485 transceivers. This interface is an excellent choice for flight controls, actuators, electro-pneumatic controllers or for similar applications of standard 1553 requiring higher data rates. The P-10SF is available as a native PMC interface or in PCI or CompactPCI formats (supplied on carrier boards). Each P-10SF PMC interface may be obtained in one or two dual-redundant channels on a PCI and cPCI carrier with front bezel or P14 (rear) I/O and optionally in ruggedized, extended operating or conduction-cooled temperature configurations.

Each interface provides BC, single RT or BM functionality with a portable, high-level API software that includes driver support for Windows and VxWorks (PPC) to reduce application development time. Standard features include -20V to 25V Common Mode Voltage Range, Bus I/O Protection to over 16-kV HBM, Failsafe Receiver for Open-Circuit, Short-Circuit and Idle-Bus Conditions and greater than 100 mV Receiver Hysteresis for the RS-485 transceivers. It also includes 48-bit message time-tagging, extensive BC and RT link-list structures, error detection, advanced BC functionality, automatic / manual RT Status Bit and Mode Code responses, along with Post, PBIT, IBIT (Built-in Tests) and cable wrap testing.

GE Fanuc Embedded Systems
Albuquerque, NM.
(505) 875-0600.
[www.gefanucembedded.com].

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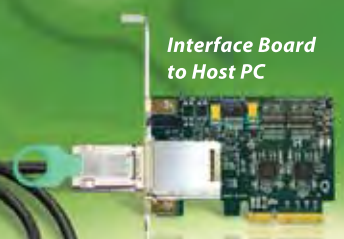
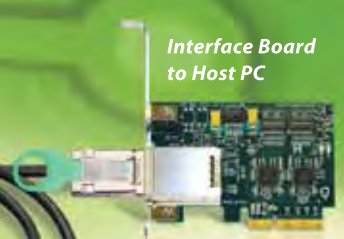


5U CPCI/CPCIe Hybrid System

Interface Board to Host PC



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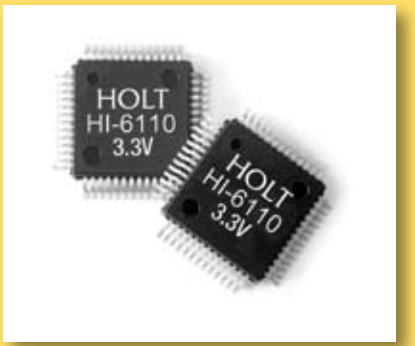
ICs Deliver 1553 Message Processing

The HI-6110 COTS MIL-STD-1553 Message Processor from Holt Integrated Circuits is a single-chip 3.3V CMOS device designed to implement the MIL-STD-1553 data communications protocol between a host processor and a dual redundant 1553 data bus. Targeting applications within the MIL-STD-1553 environment such as terminals, flight control and monitoring, instrumentation and ECCM or sensor interfaces, the HI-6110 supports MIL-STD-1553B Notice 2 and MIL-STD-1760 Stores Management. The HI-6110



includes onboard dual redundant transceivers, Manchester Encoder/Decoders, MIL-STD-1553 message-level protocol engine and sufficient on-chip data storage for single message buffering. The device dissipates less than 500 mW on-chip power at 100% duty cycle.

The HI-6110 may be configured as a Bus Controller (BC), a Remote Terminal (RT), an addressed Monitor Terminal (MT) or as a non-addressed MT. The host CPU communicates with the HI-6110 over a 16-bit parallel I/O bus. The status of message sequencing and the data transfers are flagged by pins and register bits, with registers provided for configuration, status information, error information and the type of the currently executing command. The HI-6110 is offered in either a 52-pin plastic quad flat pack (PQFP) or a 60-pin plastic chip-scale package. It will sell for $250 each in 100 piece quantities.

Holt Integrated Circuits
Mission Viejo, CA.
(949) 859-8800.
[www.holtic.com].

PMC Card Boasts Dual Redundant 1553B Links

An aircraft in flight can't afford a failure in its avionics control. That's why dual 1553 interfaces are useful. The Thales Computers' PMC-1553 provides one or two dual-redundant MIL-STD-1553B interfaces and an 8-bit TTL parallel I/O port on a single PMC module. A complete interface between a host processor and the MIL-STD- 1553B bus is implemented using an ILC-DDC BU-61688 Advanced Communication Engine (ACE) device for each channel.

The card's 1553 interfaces provide 64k x 16 bytes of shared RAM and a fully integrated MIL-STD-1553 A/B interface with Bus Controller (BC), Remote Terminal (RT) and Monitor Terminal (MT) options configurable through software. The card supports direct- or transformer-coupled interfaces and has both an internal time tag register and interrupt status register. The Bus Controller mode supports automatic retries, programmable intermessage gap times, automatic frame repetition and flexible interrupt generation.

The card's RT functionality allows RT address selection via PMC connector. Full software control is provided for RT Status and Built-in-Test (BIT) words. Double buffer and circular buffer options are programmable by subaddresses. In its Monitor Terminal configuration, three modes are provided: word monitor, selective message monitor and a combined RT/selective monitor.

Thales Computers
Edison, NJ.
(732) 494-1011.
[www.thalescomputers.com].

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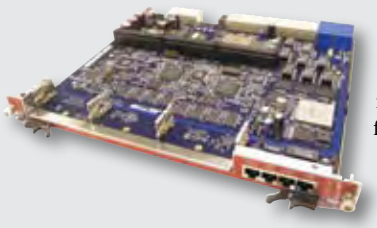


10 GbE ATCA Switch Delivers Two Separate Networks

Increasing the performance of the installed base of military communications equipment requires standardized form-factors. Now 10 Gigabit Ethernet, via ATCA 3.1, can deliver affordable improvements. To reduce time to deployment when implementing 10 GbE technology, Diversified Technology has added a highly functional, low-cost ATCA switch, the ATS1936, to their Targa line of ATCA platforms. It features three AMC sites and complies fully with PICMG 3.0 R2.0 ECN002 and PICMG 3.1 Option 1 and Option 9.

The switch can be used as hub, node or mesh-enabled board. It implements two separate switched networks on a single PCB. Separation of the base and fabric networks provides a separate control plane and data plane. The 3.0 base fabric provides 1 GbE switching and the 3.1 expansion fabric provides 1 GbE/10 GbE switching. Both networks are fully managed with a robust management suite, which reduces issues surrounding the integration of ATCA platforms with other systems. Both networks support Layer 2 switching as well as Layer 3 routing and IPv6. A single ATS1936 is priced at $5,245.

Diversified Technology, Ridgeland, MS. (800) 443-2667. [www.dtims.com].

DSPs Target Networked Apps

Military engineers building networking equipment are under a lot of pressure to improve performance while also reducing cost-per-channel. Two new DSPs from Texas Instruments, the TMS320C6424 and TMS320C6421, are designed to do just that. The company's lowest-cost C642x DSP leverages integrated peripherals, on-chip memory and high performance. With a 50% price reduction, both chips enable more than a 2.5x price/performance improvement over previous-generation DSPs. Performance of both chips peaks at 4,800 MMACs at 600 MHz. Interfaces include EDMA 3.0 with 4.8 Gbytes/s throughput and 333 MHz DDR2 memory.

Both chips are available in 400, 500 and 600 MHz versions. The C6421 provides 16 Kbytes of L1D, 16 Kbytes of L1P and 64 Kbytes of L2 SRAM, as well as two EMIF interfaces, a 16-bit 266 MHz DDR2, an 8-bit EMIFA, and interfaces for VLYNQ, McBSP and McASP. The C6424 features 80 Kbytes of L1D, 32 Kbytes of L1P and 128 Kbytes of L2 SRAM. It includes a 32-bit 333 MHz DDR2 and a 16-bit EMIFA, a PCI 33 MHz or VLYNQ interface for an optional FPGA interface and either two McBSP or one McASP interfaces. Both DSPs feature an EMAC (RMII/MII) or HPI/RMII, two UARTs, I^2C, GPIO, three PWM and two 64b-timers. Both are available in either 16 mm by 16 mm or 23 mm by 23 mm ball grid array (BGA) packaging at 0.8 mm pitch and 1.0 mm pitch, respectively. Pricing starts at $8.95 in production quantities.

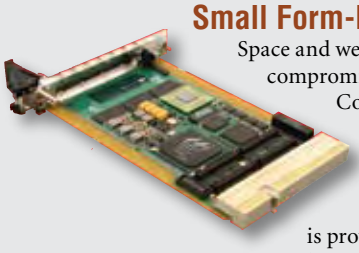
Texas Instruments, Dallas, TX. (800) 336-5236. [www.ti.com].

Virtex-II PMC I/O Modules Are Conduction-Cooled

A new series of user-configurable FPGA PMC I/O modules combines the ruggedness of conduction cooling with customizable FPGA computing for a variety of defense applications. Acromag's new PMC-CX series features Xilinx Virtex-II FPGAs with either 11k or 24k logic cells and a choice of 32 differential RS-422/485 lines or 24 RS-422/485 lines with 16 CMOS I/O channels. All models feature a 32-bit/66 MHz PCI interface and support dual DMA channel data transfers. The FPGA can generate recipe-based responses to input stimulus or function as a communications processor. Embedded multipliers for computation-intensive algorithms do not involve the CPU or an external DSP board.

Up to 1 Mbyte of configurable block RAM within the FPGA is provided along with a 256K x 36-bit SRAM. Dual-ported memory sits between the FPGA and PCI bus controller to optimize DMA data transfers. A PLX PCI9056 device handles system connectivity with a high-performance interface to the PCI bus. Acromag's Engineering Design Kit includes a compiled FPGA file and example VHDL code. Acromag's ActiveX (OLE) controls software package functions as drivers for compatibility with Microsoft Visual C++ and Visual Basic. C libraries for VxWorks, QNX and other operating systems are available. Prices start at $2,600.

Acromag Embedded Board Group, Wixom MI. (248) 624-1541. [www.acromag.com].



Small Form-Factor Board Expands I/O Flexibility

Space and weight constraints for embedded technology in military and aerospace applications have created difficult compromises between size and a full complement of I/O. The SCP/DCP-124P from Curtiss-Wright Controls Embedded Computing takes advantage of the compact 3U CompactPCI SBC format and I/O flexibility to overcome these challenges. Utilizing PICMG 2.3, the SCP/DCP-124P routes I/O signals and supports mapping of PMC I/O through the backplane. It features Freescale's Altivec-enhanced 7448 PowerPC supported by 1 Mbyte of internal ECC L2 cache running at core processor speed and up to 1 Gbyte of ECC DDR SDRAM.

The board's cPCI bus operates at 33/66 MHz and supports both 3.3V and 5V signaling. System expansion is provided by an onboard 64-bit, 100 MHz PCI-X-capable PMC site. The SCP/DCP-124P is available in both conduction-cooled and air-cooled versions with optional rear transition cable sets to facilitate system integration and development. Pricing starts at $6,030.

Curtiss-Wright Controls Embedded Computing, Leesburg, VA. (703) 779-7800. [www.cwcembedded.com].

Battery Management System Supports Li-Ion

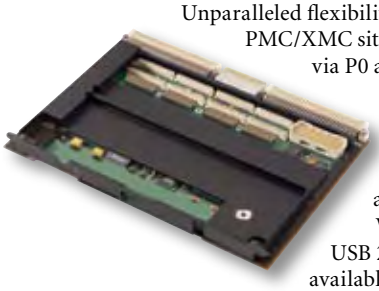
Portable battery-power devices represent one of the most dynamic areas of military system design these days. OceanServer Technology has introduced a patented, fully engineered battery and power system that lets designers add smart, rechargeable Li-Ion battery back-up power as an OEM component to virtually any type of electronic and electromechanical equipment. The Intelligent Battery and Power System serves as a complete AC/DC power supply and provides clean, regulated DC, sourced from Li-Ion battery packs, an AC wall outlet or any external DC source including solar and wind power. Seamlessly taking over if the external power is interrupted, it recharges automatically when the power is restored and provides status feedback such as charge and discharge rate, time to empty and number of active batteries.

Modular, fully scalable and SMB compliant, the Intelligent Battery and Power System lets designers speed the development cycle of integrating up to 48 VDC battery power into an OEM product. A variety of battery management modules and DC converters are offered that can manage up to eight packs each, to provide up to 760 watt-hours of high-density Li-Ion power. The Intelligent Battery and Power System is priced starting at $299, depending upon power requirements.

OceanServer Technology, Fall River, MA. (508) 678-0550. [www.ocean-server.com].

VME SBC Blends Dual Core CPU, 4 GB of RAM

This is shaping up to be the year of dual-core-processor based SBCs. Exemplifying that trend, GE Fanuc Embedded Systems has announced the PPC9A, the latest addition to the company's PowerXtreme family of 6U VME single board computers. At the heart of the PPC9A is Freescale's latest PowerPC processor, the dual-core 8641D operating at 1.3 GHz. The PPC9A—which is 2eSST-capable—supports up to 4 Gbytes of DDR2 memory, and up to 1 Gbyte of flash memory.



Unparalleled flexibility is provided through the provision of not only two PMC/XMC sites (PCI-X 133 MHz/8-lane PCI Express) supporting I/O via P0 and P2, but also GE Fanuc's unique AFIX (Additional Flexible Interface Xtension) site that allows custom functionality to be added to the board at minimum cost and in minimum time. Standard AFIX modules for graphics, SCSI, 1553, digital I/O and flash memory are also available.

With two Gbit Ethernet 10/100/1000 Base-T ports, two USB 2.0 ports and six serial ports, the PPC9A—which is available in five air- and conduction-cooled variants—is highly specified in terms of communications and I/O, while the provision of up to 1 Gbyte of write-protectable flash memory, 128 Kbytes of non-volatile RAM with Autostore and a Serial ATA disk interface means that storage is equally well catered to.

GE Fanuc Embedded Systems, Albuquerque, NM. (505) 875-0600. [www.sbs.com].

VXS Board Offers Six 160 MS/s ADC Channels

High-density processing is the watch word for military designers developing advanced signal generation solutions in applications such as radar, electronic warfare and mobile communications. For just such applications, TEK Microsystems has announced the new Tarvos VXS, the first VXS product to combine six channels of 16-bit, 160 Msample/s analog to digital conversion with FPGA-based DSP processing technology in a single slot along with a single digital to analog conversion output channel.

In a ANSI/VITA 41.0 VXS Payload card form-factor, the board's analog to digital converters are linked into a Xilinx FPGA equipped with an advanced double data rate SDRAM memory architecture with a capacity of up to 5 Gbytes on a single card. FPGA also supports high-speed off-board communications through two front panel high-speed serial ports or eight high-speed serial links over the VXS standard P0 connector onto the backplane using protocols such as Gigabit Ethernet, VITA 55 / Aurora, Serial RapidIO, Serial FPDP, etc., programmable via firmware. The Tarvos VXS is available now and pricing starts at $19,900 for single unit quantities.

TEK Microsystems ,Chelmsford, MA. (978) 244-9200. [www.tekmicro.com].

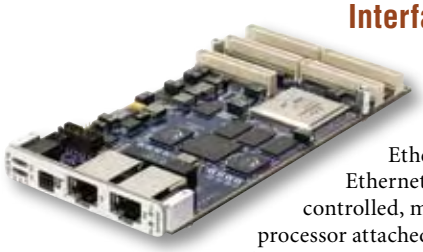
18-Slot Chassis and Board Family Supports PXI Express

The emerging PXI Express standard builds on commercial PCI Express technology to expand the applications served by the multivendor PXI standard, and military test and instrumentation engineers are itching to make use of it. Helping make that happen, National Instruments has announced the industry's first PXI Express high-speed instruments as well as the industry's first 18-slot PXI Express chassis. The new modular instruments include the NI PXIe-5122 100 Msamples/s, 100 MHz dual-channel digitizer and the NI PXIe-6537 and NI PXIe-6536 50 MHz and 25 MHz 32-channel digital I/O modules. The NI PXIe-1065 18-slot chassis (shown) offers up to 1 Gbyte/s per-slot dedicated bandwidth and a combination of both PXI and PXI Express slots.

The NI PXIe-1065 18-slot chassis complements the existing NI PXIe-1062 8-slot chassis to address higher-channel-density PXI Express-based systems. The new chassis includes a combination of PXI and PXI Express hybrid slots to accept a mix of both existing PXI modules and high-bandwidth PXI Express modules. All of the new products integrate with a variety of software including the NI LabVIEW graphical development environment, LabVIEW SignalExpress interactive measurement software and NI TestStand test management software.

National Instruments, Austin, TX. (512) 683-0100. [www.ni.com].

Interface Connects Wideband Sensors, GbE Nets



Traditionally, wideband sensors could not be directly connected to military networks based on 1 or 10 Gigabit Ethernet, reducing their use in the most demanding real-time system applications, such as radar, data acquisition and SIGINT. The bidirectional Sensor Link SLX101 interface from Critical I/O connects wide-band I/O devices such as A/D converters, digital receivers and imaging devices with standard Ethernet networks in a CMC form-factor. It converts sensor data streams to or from standard UDP or TCP Ethernet data at up to 320 Mbytes/s. The plug-in replacement for FPDP and serial FPDP CMC modules can be controlled, managed and monitored—and data streams can be rerouted—through the same Ethernet network by any processor attached to the network.

The SLX101 CMC requires no software or intelligence at the sensor. Since it is self-contained with no host processor, sensor data can be streamed at wire-speed with very low latency. Data can be sent to a host of devices connected to the Ethernet network, such as signal processors, workstations, storage devices or other Sensor Links. The SLX101 features dual 1 GbE interfaces and flexible FPDP, LVDS or custom sensor interfaces, as well as optical and copper Ethernet connectivity, an integrated Ethernet protocol offload engine and integrated hardware BIT. Pricing in production quantities is $3,990.

Critical I/O, Irvine, CA. (949) 553-2200. [www.criticalio.com].

VME Microwave Tuner Delivers Fast Switching, Low Noise

Uncoupling tuning speed from phase noise has created a very fast, high-performance microwave tuner suited for SIGINT and electronic warfare systems. The Echotek 1800 GT ultra high-performance wideband microwave receiver from Mercury Computer Systems features a direct digital synthesizer to achieve this uncoupling. It consists of two single-slot VME modules that form a microwave down-converter tunable over the entire 0.5 GHz to 18 GHz range, providing both narrowband and wideband outputs. Simultaneous analog outputs of 80 MHz and 500 MHz are centered at 160 MHz and 1 GHz, respectively.

The functional separation of RF and synthesizer functions makes the Echotek 1800GT equally suited for single-channel and multi-channel phase-coherent systems, including beamforming and phase interferometry for direction finding. A direct digital synthesis architecture offers fast frequency agility and eliminates the tuned frequency overshoot or undershoot associated with traditional analog PLL designs. Integrated phase noise is <0.5 degrees RMS at 18 GHz. Digital circuits used to implement signal processing do not suffer the effects of thermal drift, aging and component variations associated with their analog counterparts, so no temperature compensation is necessary in the tuner, allowing more repeatable and predictable performance. Pricing is $92,000, and volume discounts are available.

Mercury Computer Systems, Chelmsford, MA. (978) 256-1300. [www.mc.com].

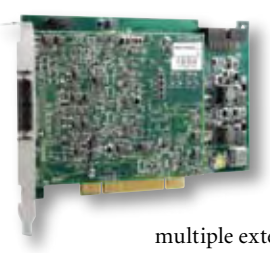
ARINC 429 Avionics Bus Interfaces Offer 12 Channels

Developers working in aviation applications that measure and control parameters such as pressure, stress/stain, vibration and temperature often need to combine analog and digital measurements. The DNA-429-5xx series of ARINC 429 avionics bus interfaces from United Electronic Industries features 12 channels each in three different configurations. The DNA-429-566 offers 6 Tx/6 Rx channels, the DNA-429-512 provides 12 Rx channels and the DNA-429-548 has 4 Tx/8 Rx channels. All boards are software-selectable for high-speed (100 kHz) or low-speed (12.5 kHz) operation.

Receive channels include automatic label filtering so only data from selected channels is captured. The filter may be set to forward data from between one and 255 labels, or may be disabled so all data is captured, regardless of source. Transmit channels may be set to transmit asynchronously or based upon a hardware-controlled scheduler. Software is provided as part of the UEIFramework, which delivers an API that supports Windows, Linux and most RTOSs, including QNX, RTX and RT Linux. It also supports LabVIEW, MATLAB/Simulink, DASYLab or applications that support ActiveX or OPC servers. Pricing is $3,000 each.

United Electronic Industries, Canton, MA. (781) 821-2890. [www.ueidaq.com].

PCI, PXI Data Acquisition Cards Boast Higher Throughput/Channel



Modular test architectures such as PXI let military system designers create synthetic instrumentation systems that can replace a host of traditional digital equipment. ADLINK is smoothing the way with its latest high-sampling, multi-function PXI-2016 data acquisition card, also available in a PCI form-factor, the DAQ-2016. Both cards feature a maximum transfer rate of 800 ksamples/s per channel and are designed for large-scale data collection. The four-channel cards offer 16-bit resolution, as well as a variety of analog and digital trigger sources and modes for multi-channel simultaneous sampling efficiency.

To support channel count expansion using an external clock, the DAQ-2016 and PXI-2016 cards can synchronize multiple external devices using a System Synchronization Interface or a PXI trigger bus. The cards deliver two 12-bit, 1 Msample/s analog output, 24-channel programmable DIO and two 16-bit timers/counters that provide flexibility for multitasking. Included are a WDM driver for C/C++, VB, Delphi, C++ Builder and .NET programming languages and full device drivers for MATLAB and LabVIEW. Pricing for the DAQ-2016 and PXI-2016 starts at $1,495 and $1,695, respectively. Volume discounts are available.

ADLINK Technology America, Irvine, CA. (949) 727-2077. [www.adlinktech.com].

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PMC Compute Nodes Boast Over 156k FPGA Slices

FPGAs are making a dramatic difference in military signal processing applications, allowing several general-purpose processing nodes to be replaced with a single FPGA-based node. That helps reduce board slot count, while shrinking overall cost and power consumption. Leveraging that trend, Micro Memory today introduced the MM-7105, MM-7110 and MM-7115 CoSine FPGA PMC Compute Nodes. The company claims these to be the first PMCs to offer over 89k FPGA slices, with certain configurations exceeding 156k FPGA slices as well as the first PMCs to include over 600 Xtreme DSP slices.

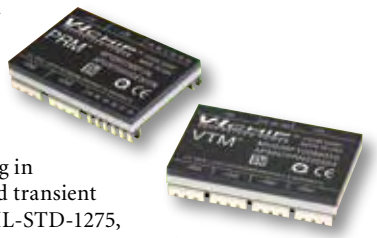
The MM-7105 is the first rugged PMC to include the powerful V-4 LX200 FPGA from Xilinx, while the MM-7110 is the first PMC to combine the LX200 with a SX55, and the MM-7115 is the first PMC to combine the LX200 with a LX160. The optional CoSine bitstream consists of a PCI/PCI-X bus interface, specialized PCI DMA engine, UPL DMA engine, and multi-ported DDR II memory controller with ECC. The MM-71xx series is offered in rugged convection-cooled "DR" models and rugged conduction-cooled "DT" models that each operate at temperatures of -40° to +71°C. Quantity one list pricing for the MM-71xx series is $16,000.

Micro Memory, Chatsworth, CA. (818) 998-0070. [www.micromemory.com].

28V DC-DC V·I Modules Aim at MIL-COTS Apps

Size and weight are a big deal for power systems in mission-critical portable and airborne applications. With that mind, Vicor has announced the availability of MIL-COTS 28V DC/DC V•I Chip modules. This new product line consists of a 28 VDC input PRM regulator and a family of VTM current multipliers with output voltages from 1 to 50 VDC. Each module weighs only 0.5 oz. or 15g and measures just 1.28 x 0.87 x 0.26 inches.

A PRM and VTM chipset can provide up to 100A or 115W for a system density of 172 A/in³ or 198 W/in³, and because the PRM can be located, or factorized, remotely from the point of load, these current and power densities can effectively be doubled at the load itself. The modules may be paralleled for higher power arrays. A compatible filter (M-FIAM7) is available that provides EMI filtering in compliance with MIL-STD-461 and transient suppression in compliance with MIL-STD-1275, MIL-STD-704 and DO-160. The MIL-COTS PRM and VTM chipsets are available for less than $170 in OEM quantities.



Vicor, Andover, MA. (978) 749-8359. [www.vicorpower.com].

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XMCs Serve Up 1.5 and 3 Gbit/s A-D Conversion

Demanding real-time applications such as Electronic Counter Measures (ECM) and radar have an endless appetite for the blend of high-speed analog input and high-performance FPGA processing. Feeding that appetite, VMETRO has announced two high-speed analog input XMC modules with the latest generation Xilinx Virtex-5 FPGA. The AD3000 is a single-channel 3 Gsample/s ADC, and the AD1500 is a dual-channel 1.5 Gsample/s ADC. The modules' analog input utilizes either a National Semiconductor ADC083000 or ADC081500 8-bit converter. Both designs share a common FPGA back-end with either a Virtex-5 SX95T or LX110T FPGA and are directly connected to the analog input.

An LVPECL trigger input, an LVPECL output, an LVTTL output and the sample clock input are provided on the front panel. Off-board data links are provided through either PCI-X or PCI via the PMC connectors or high-speed, multi-Gbit/s Virtex-5 RocketIO transceivers using the XMC connectors. Both the AD3000 and the AD1500 will be available in XMC and PMC form-factors, for air- and conduction-cooled environments. Available Q3 2007, pricing for the AD1500 and AD3000 starts at $13,995.

VMETRO, Houston, TX. (281) 584-0728. [www.vmetro.com].

PCI Express x4 Card for Laptops Does 2.5 Gbits/s

It used to require a big rack of boards to craft military test equipment. There was no other way to get the bandwidth and I/O breadth needed for complex system tests. Now that same functionality can be offered even at the laptop computer level. Along those lines, One Stop Systems has released its PCI Express (PCIe) x4 Express Card, enabling laptops to operate with high-speed expansion capabilities at 2.5 Gbits/s to a x4 downstream device including an expansion chassis or storage system. Other standard Express Cards on the market only allow connection to the x1 PCIe cable. The PCIe x4 cable downlink connects to all One Stop Systems' expansion chassis for additional add-in board capacity. The Express Card connects to a downstream device through a PCIe x4 cable.

Key features of the PCIe x4 Express Card include LVPECL Spread Spectrum reference clock buffer outputs, electrical isolation at cable connector, low power and a powered cable connector for cables requiring active equalization for additional distance. The Express Card does not require software drivers and supports up to 7-meter passive and 25-meter active cables based on the PCIe Cable standard. The PCIe x4 Express Card lists for $496 and is available immediately.

One Stop Systems, Escondido, CA. (760) 745-9883. [www.onestopsystems.com].

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Isolated USB Modules Optimized for Harsh Duties

USB has all but taken over as the key interface bus for data acquisition. Offering a product optimized for use in harsh environments, Data Translation has announced the DT9853 Series of low-cost USB bus-powered D/A modules. Contrary to the popular use of USB modules in benign lab-type applications, the DT9853 series is galvanically isolated to +/- 300V and provides voltage as well as the industrial standard 0 to 20 mA current outputs concurrently. These modules operate as high-speed USB devices for maximum speed and accuracy.

The DT9853 Series is ideal for process control, control loop and test applications requiring stable and accurate output signals. The plug and play installation of these USB modules simplifies configuration and reduces set-up time while offering unrivaled isolation and superior accuracy. The unit provides 4 or 8 glitchless analog outputs with 16-bit resolution for highly accurate measurements. Eight dedicated digital input lines and 8 dedicated digital output lines are provided for external event synchronization. The DT9853 Series of isolated D/A modules for USB is priced starting at $495.

Data Translation, Marlboro, MA. (508) 481-3700. [www.datatranslation.com].

Pentium M Board Boasts Six Gbit Ethernet Ports

The military continues to embrace Ethernet as a means of system connectivity. Feeding that need, WIN Enterprises has announced the MB-06067, a high-performance control board designed for Unified Threat Management (UTM) and other networking applications. Using either the Intel 82541PI or Intel 82551ER Ethernet controller, the new board supports six Gbit Ethernet copper or 10/100 LAN ports with optional bypass function on two ports. The control board uses an Intel Pentium M or Celeron M processor with Intel 852GM express chipset and ICH4 I/O controller. It supports system memory up to 1 Gbyte with one DDR memory socket. Both CompactFlash and memory can be replaced.

OEMs can work with WIN Enterprises to develop purpose-build security appliances based on the MB-06067. Standard chassis and unique bezel designs for product branding enable fast time-to-market with individual products or entire product lines. The board also features two serial ports, one parallel port, three USB 2.0 ports, one E-IDE connector and one CompactFlash type II socket. The PCI golden edge fingers support two PCI slots. Digital I/O support includes four input and four output lines. The MB-06067 versions are available now and pricing ranges from $356 to $395 for one unit, depending on configuration and options.

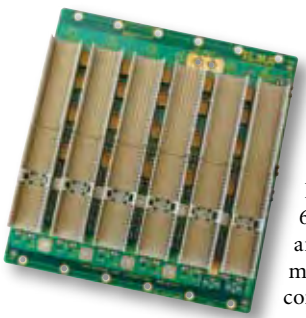
WIN Enterprises, North Andover, MA. (978) 688-2000. [www.win-ent.com].

Synchro/Resolver Converter Comes on PC/104 Card

Combined with analog and digital I/O, synchro/resolver converters provide a complete system solution for radar position tracking. A new, highly accurate, six-channel, programmable synchro/resolver-to-digital converter from North Atlantic Industries on a PC/104 card reduces size, complexity and cost. It also possesses continuous built-in-test functions and digital velocity outputs. The DSP-based 73SD4 includes six independent, transformer-isolated, programmable synchro/resolver tracking converter measurement channels. Each channel has 16-bit resolution, ±1 arc-minute accuracy, a tracking rate of up to 150 RPS, accurate digital velocity output, incremental encoder (A+B) outputs and wrap-around self-test.

Channel pairs can be programmed for any speed ratio between 1:1 and 255:1. The 73SD4 requires a single +5 VDC power supply, operates over a frequency range of 47 Hz to 10 KHz and has an auto-ranging input range of 2 Vrms to 28 Vrms. Each unit includes 16 programmable digital input/output channels, a latch feature for reading all channels simultaneously and an optional programmable excitation reference supply. Continuous background built-in-test is provided on all functions and channels, including reference and signal loss detection, and each channel is self-calibrating. Operating temperature range is -40° to +80°C. Pricing for 100 pieces is $2,500 each.

North Atlantic Industries, Bohemia, NY. (631) 567-1100. [www.naii.com].



3U 32-bit CompactPCI Backplane Offers More I/O

A new 3U 32-bit CompactPCI backplane in a six-slot size from Elma Bustronic offers hundreds of I/O pins across the backplane. In the 64-bit version, these pins are defined and therefore unavailable for use by military engineers. The backplane is compliant with the latest PICMG specifications and utilizes a controlled-impedance stripline design, eliminating nearly all crosstalk.

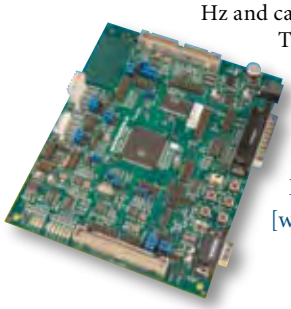
The Bustronic 32-bit backplane line currently includes a 6U eight-slot version and 3U versions in three, six and eight slots. A wide range of 64-bit cPCI backplanes and PICMG 2.16-compliant packet switching lines are also available, as well as various other CompactPCI accessories. Pricing for the six-slot 3U 32-bit CompactPCI backplane starts at under $300.

Elma Bustronic, Fremont, CA. (510) 490-7388. [www.elmabustronic.com].

Image Stabilization System Features Zero Loss

In various types of mobile-, ground-, air- or space-based observation platforms, such as reconnaissance aircraft and UAVs, camera images must be stabilized for accurate viewing without losing either field of view or resolution. A new compact, fully automatic image stabilization system from Energen does exactly that. The Energen Image Stabilization System consists of a gyrosensor that measures vibration, a lens assembly with a CCD, a DSP and resident software to provide fully automatic operation.

Featuring zero loss in resolution or field of view, it operates by sensing vibration and counteracting its effect via software-controlled optical elements so that the CCD effectively sees a high-resolution image. The Energen Image Stabilization System handles vibrations of up to 100 Hz and can achieve image stability to 35 µrad.



The system, including software, can be packaged to meet specific OEM requirements. It is priced from $4,995, depending on configuration and quantity.

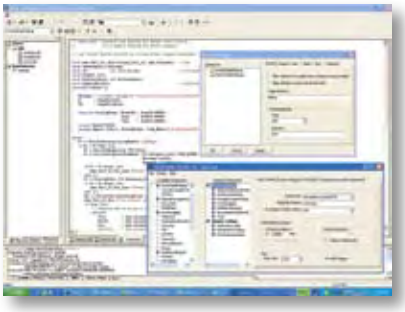
Energen, Lowell, MA. (978) 259-0100. [www.energeninc.com].

PC-Based Data Recorder Achieves 400 Mbytes/s Sustained

A high-speed, portable, PC-based recorder that's also reliable and rugged enough for use in the field is high on the wish list of engineers working in many defense applications. Housed in a rugged portable chassis, the Big River P440 data recorder from Conduant achieves over 400 Mbytes/s of sustained recording or playback performance in a portable, self-contained unit. It features an Intel Core 2 Duo processor, Gigabit Ethernet connectivity and expansion PCI slots for optional third-party high-speed acquisition I/O boards. It includes a high-resolution, flat panel screen display, keyboard with touchpad mouse and support for FPDP, LVDS and Serial FPDP (optical) interfaces. Capacities of up to 3.2 Terabytes are available.

The P440 data recorder incorporates Conduant's StreamStor Amazon SATA disk controller, as well as 16 high-capacity 2.5-in. notebook disk drives. The disk controller utilizes a wide range of popular interface options such as FPDP, Serial FPDP, FPDP II, LVDS or the PCI bus for direct-to-disk recording and features data forking and circular buffer recording. Pricing for the Conduant ranges from $35,000 to $40,000.

Conduant, Longmont, CO. (303) 485-2721. [www.conduant.com].



ObjectAda Ported to ETS RTOS Version 13

Ada continues to be an important software language particularly for safety- and mission-critical applications. Serving that need, Aonix has ported ObjectAda V8.2 to the latest Ardence ETS RTOS. This advanced version of ETS, Version 13, offers many new features, including kernel-level memory protection—a critical feature for military system developers who need to bring real-time, secure memory applications into the Windows environment.

Ardence's Phar Lap ETS, a hard real-time RTOS designed for applications targeting execution on x86-based platforms, now boasts improved connectivity support. With this edition, ETS delivers TCP/IP multicast support and complete access to ETS TCP/IP APIs enabling development of network drivers and for support of higher layer protocols. The Aonix ObjectAda for Windows brings the improvements of ObjectAda 8.2 to the Windows development platform. In integrating current Windows improvements with the Aonix Ada 95 compiler, Aonix has delivered enhancements to the object code and symbolic debugging information generation and provided full compatibility with the Microsoft Visual Studio .NET 2003 development tools. ObjectAda for Windows targeting Ardence ETS is available immediately and is priced starting at $15,499 per seat with volume discounts available.

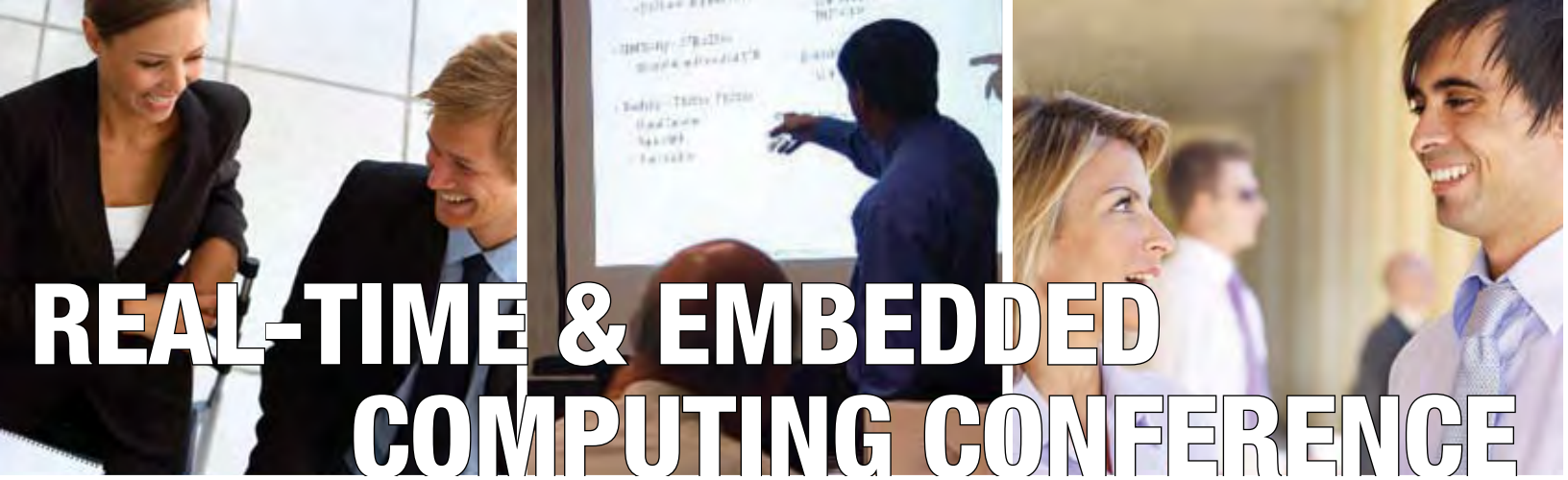
Aonix, San Diego, CA. (858) 457-2700. [www.aonix.com].

2.8 GHz Mini-ITX Board Sports Six Serial Ports

Today's level of computer integration allows a tremendous amount of computing power to fit a stand-alone board. That's driven some military applications to consider form-factors like the Mini-ITX motherboard form-factor. Serving that need, the eAutomation Group of Advantech introduces the AIMB-240, a Mini-ITX motherboard with 2.8 GHz processing power and six serial communication ports. It's equipped with a 82852GME chipset, supports Pentium 4 and Celeron processors, and has 400/533 MHz FSB and 1 Gbyte of DDR 266/333 SDRAM. With Intel's integrated Extreme Graphics 2 controller, the AIMB-240 delivers integrated 3D graphics and video capability without adding expensive graphic cards. There are multiple display interfaces such as LVDS, DVI, TV-out and CRT as well as multimedia features including 5.1 multi-channel audio and DVI transmission of 135 mega-pixels per second.

The AIMB-240 uses the Intel ICH 4 to enable expandability. There's one 32-bit/33 MHz PCI slot and one 32-bit/33 MHz mini-PCI slot that enables flexible expansion. The six serial communication ports and six USB 2.0 ports offer superb connectivity for keyboards, mice, and other peripherals. The motherboard also supports dual 10/100Base-Tx Ethernet. Pricing for the AIMB-240 starts at $219.

Advantech, eAutomation Group, Cincinnati, OH. (513) 742-8895. [www.eAutomationPro.com].



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- *SIGINT System Architectures.* The impact FPGA advances have had on signal intelligence (SIGINT) is no less than staggering. Enabled by advances in FPGA technology, configurable computing at the system level has matured quickly over the last couple of years to where it's the preferred choice for deployment in signal-processing-intensive systems such as SIGINT. Whether the signal in question is audio, visual, radar or other medium, the systems typically use several algorithmic components, each suited for different processing devices, such as FPGAs, DSPs and general-purpose processors. This feature section delves into the board- and system-level solutions for signal intelligence and technologies enabling them.
- *Future Combat Systems Update.* The Army's Future Combat Systems (FCS) program ranks as one of the most complex ever taken on. Comprised of a wireless data network using advanced communications technologies, FCS links soldiers with several new, lightweight manned and unmanned ground vehicles, unmanned aircraft, sensors and weapons. This feature updates readers on the status of the FCS program, with a look at the central role that embedded computing architectures like cPCI and VPX are expected to play.
- *Shock & Vibration for Boards and Enclosures.* As systems get more dense and complex, the problem of engineering boards and enclosures isn't getting any easier. Meeting the stringent levels of shock and vibration ratings required by most defense and aerospace programs is no slam dunk. Relying on outdated Mil-Spec guidelines like MIL-STD-810F is no longer sufficient, and full environment stress screening techniques like HASS and HALT have moved into the forefront. Articles in this section delve into those areas and compare the solutions available.
- *Avionics I/O.* Technology choices in avionics I/O aren't as simple as they used to be. The 1553 interconnect is found in almost all existing military aircraft and is still being designed into new aircraft. But it's no longer the only game in town. For some weapons systems, 1553's connectors are too big, and for radar, it's too low bandwidth. Higher-speed interfaces like 1394b for flight controls and Fibre Channel, Gigabit Ethernet or AFDX for mission systems are among the options getting mindshare among avionics system designers. This section compares these alternatives, with a look at the various mezzanine card products that support them.

COTS

Editorial

Jeff Child, Editor-in-Chief

In our special supplement on Payloads for UAVs in the issue, Jon Lathrop of Mercury Computer Systems makes a good analogy comparing today's U.S. UAV industry with this country's jet aircraft industry of the 1950s. Then as now, fairly new technology was being applied and evolved to where it became widely used, but was extremely non-standard. The result is a lot of expensive duplication of effort and resources.

A report to Congress by the Government Accountability Office (GAO) last month raised the standards and collaboration issues in the context of the DoD's management and integration of Intelligence, Surveillance and Reconnaissance (ISR) assets, in which UAVs play a major role. UAVs, like the Air Force's Global Hawk and Predator and the Army's Hunter, are among the sources intelligence data that are part of ISR.

Attempts to leverage common aspects of UAV programs across the Service Branches have been mixed, although not without some successes. At times the Services have initiated collaborative approaches with each other on their own. At times they've resisted or avoided collaboration with another branch.

Taming the Wild UAV West

Among the more successful UAV collaboration efforts is the Army and Navy's development of the Fire Scout. As part of the Future Combat Systems program, the Army began developing in 2000 a vertical takeoff and landing UAV called Fire Scout. On their own initiative, Program managers from the Army Fire Scout contacted their counterparts in the Navy Fire Scout program to share information and look for any synergies between the two programs.

Army and Navy officials met several times to discuss configuration, performance requirements, testing, support, and other issues. And while at first the requirements for the two systems were quite different—the Army's UAV had four blades and a larger engine, while the Navy's system had three rotor blades and a smaller engine—after some discussions, the Navy decided to switch to the Army's configuration. As a result the two branches are now acquiring common components—such as the air vehicle and flight components—for their Fire Scout UAVs.

Thanks to their collaboration, estimated savings to the Army in research and development alone is about $200 million. Moreover, as both programs mature, it's expected that more savings could be realized through contract price breaks on quantities and sharing test efforts—test vehicles, support equipment, and test components. Acquisition of common hardware under one contract will also reduce procurement administrative lead time and permit common design, tooling and testing. Meanwhile, development pf future payloads—for communications, sensors and data links—could all be bought jointly.

Another case where there's opportunity for collaboration between the Branches is new Broad Area Maritime Surveillance (BAMS) program. BAMS released a request for proposals in February and plans to proceed with system development and demonstration in October. BAMS serves as a UAV adjunct to the Navy manned Multi-mission Maritime Aircraft (MMA) platform.

After analyzing various UAV alternatives for the BAMS program, the front runner appears to be the Global Hawk. For the demonstration phase the Navy procured two Global Hawks and associated ground controls and gear. The demonstration program is expected to leverage the existing Global Hawk system to develop tactics, training and techniques for maritime mission applications. If the Global Hawk is selected for the deployed program, there are opportunities for the Navy to work with the Air Force and leverage its knowledge, along with some of the same collaboration and sharing of costs enjoyed on the Fire Scout programs.

Fortunately the future is wide open for BAMS and its chance to reap the benefits of inter-branch collaboration. In contrast the Warrior and Predator programs missed some of theirs. Reportedly the Air Force and Army repeatedly resisted collaborating on their Predator and Warrior UAVs. A legacy program, the Air Force's Predator has been operational since 1995. The Predator's persistent surveillance/full motion video capability ranks as a valued asset with proven success. But when the Army began in 2001 to define requirements for the Warrior—a system similar to the Predator—it did not explore potential synergies between it and the Air Force program. Reportedly, concerns were raised about duplication of an existing capability, but to no result.

In January of last year, responding to direction from the Quadrennial Defense Review and the Secretary of Defense, the Army and Air Force agreed to consider cooperating on the acquisition of the two systems. Part of the issue with the Warrior and Predator is that the Army and Air Force have different concepts of operation and requirements. For example, the Army does not agree with the Air Force's requirement for rated pilots. The two branches are now working to address that gap. The Air Force plans to acquire two of the more modern Warrior airframes and test them. Later, the Services intend to compare their requirements for ground control stations and automated takeoff and landing.

One effort the DoD is making to address these common design challenges going forward is to apply the Joint Capability Portfolio Management concept to ISR systems across DoD as a test of the concept. That effort seeks to develop and manage ISR capabilities across the entire department—rather than by military service or individual program—and by doing so, enable interoperability of future capabilities and reduce redundancies and gaps. Better to think in terms of collaboration from the ground up than trying to integrate 25 or 30 separate programs, buried in each of the Services' budgets, late in the design cycle. ▮▮

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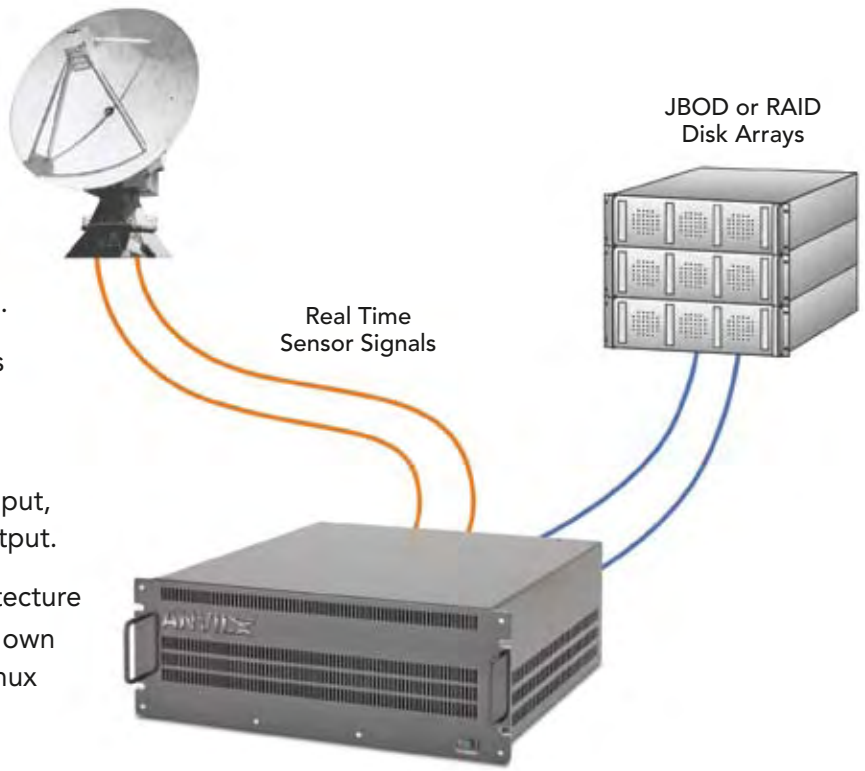

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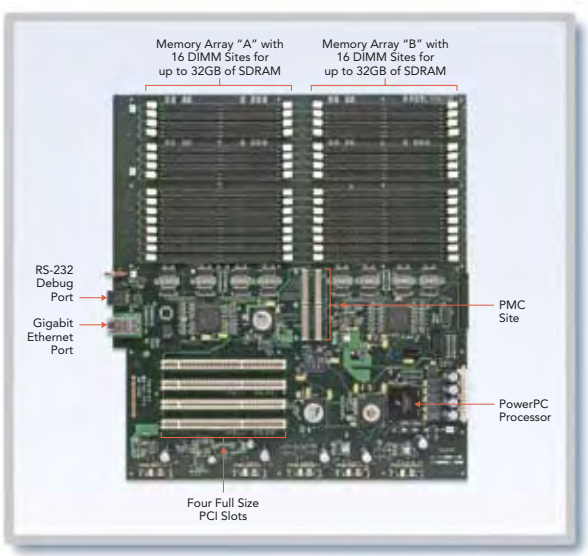

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